AsA LAUGHTON

Formerly KCS 5290
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Technical Training

AN/TSC-60 Communications Central

O/L (407L)

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USAF TECHNICAL TRAINING SCHOOL
3410th Technical Training Group
Keesler Air Force Base, Mississippi

All Blocks

Designed For ATC Course Use

ATC Keesler 5-3516

CONTENTS

Supersedes KCS 5290, dtd September 1977, which may be used.

GLOSSARY

A	Accessible Memory Address 1 (WT1)
ACC	Accumulator Clock
ACD	Accumulator Input Bar
AL1	Monitor Storage Address Line 1 (WT8)
AL2	Monitor Storage Address Line 2 (WT4)
AL3	Monitor Storage Address Line 3 (WT2)
AL4	Monitor Storage Address Line 4 (WT1)
ANR	Address Shift Signal (Address Not Required)
ARC	Address Select Clock (Address Recognition Clock)
B	Accessible Memory Address 2 (WT2)
BCD	Binary Coded Decimal
BNZ + CNZ + COZ	Conditional branch test signal
BPZ	Branch Indirect Bar
BR	Branch Bar
C	Accessible Memory Address 3 (WT4)
CA	Radio Counter State A
CB	Radio Counter State B
CCCS	Communications Computation Control System
CLL	Clock, Logic Level
COZ + BNZ + CNZ	Branch Signal
CRA	Radio Counter Address bit 1
CBR	Radio Counter Address bit 2
D	Accessible Memory Address 4 (WT8)
DBC	Data Bank Clock
DBI	Data Bank Input
DCFE	Device Control Functional Element
DCU	Device Control Unit
DBO	Data Bank Output
DBOT	Data Bank Output Retimed (4800 Bits/Sec)
DBT	CCCS Control Data
DELIM	Delimiter
DIA	Dialogic Reference
DR	Data Register
EA1	Address Enable 1 (DCU 0)
EA2	Address Enable 2 (DCU 1)
EA3	Address Enable 3 (DCU 2)
EA4	Address Enable 4 (DCU 3)
EA5	Address Enable 5 (DCU 4)
EA6	Address Enable 6 (DCU 5)
EA7	Address Enable 7 (DCU 6)
EA8	Address Enable 8 (DCU 7)
EEL	Logic Level Address Enable

EMB	Accumulator Clock Enable
EXP	Expander Output
FD	Fault Register Output
FI	Fault Data In
FIC	Fault Data Clock
FINS	Fault In Instruction Register
FL	CCCS Fault Inhibit (Fault Load)
IAC CLOCK	Instruction Address Counter Clock
IAC LOAD PULSE	Instruction Address Counter Load Pulse
IDRT	Process Time Interval Signal (Internal DR Timing)
IDS	Input CCCS Data Signal
INC	Instruction Storage Clock
LCD	Literal Code Signal
LL	Logic Level
LLA	Logic Level Address
MDO	Memory Data Output
OPO	Operator Output
OUTS	Output Sine Wave
PI	Power Interrupt
01	Phase 1 Clock
03	Phase 3 Clock
RCT	Return Control Transfer
ROM	Read Only Memory
ROTE	Rotate Enable
RST	Seset
S1	Accumulator Serial Output/ CCCS Subaddress 1
S2	CCCS Subaddress 2
SDT	Set for Data Transfer
SWO	Logic Level Input Bus (Slave Word Output)
STR-F	Store Fault Data
SYNC (LL DELIM)	Logic Level Delimiter Bus
$\overline{\text{SYNC (LL DELIM)}}$	
TCSC	CCCS Timing Input
WT	Weighted Numeric Value
YN	Logic Level Sync Enable
Z2	Memory Address WT 1024