Chapter 10

CONTROL HEAD WORDS
(Logic Level)

LOGIC LEVEL BUS. The logic level bus is the interface between the computer and the transmit and receive control heads. This bus consists of four pairs of wire commonly called the control bus, the monitor bus, the clock bus, and the delimiter bus. The data transferred via these buses is in serial word formats, the composition of which is described in subsequent paragraphs. Data is transmitted from the computer to the transmit and receive control heads by the control bus, and the monitor bus transfers data from the two control heads to the computer. The clock and delimiter buses are driven by computer processor card A7A4 and provide bit timing and word timing respectively. Figure 10-1 shows the relationship between the signals on the four buses that make up the logic level bus, and the following descriptions explain the functional character of these signals.

Clock Bus. The clock bus is a continuous square-wave signal symmetrical to within plus or minus 5 percent. This signal is used as an internal timing reference and is generated by processor card A7A4. A data transfer rate of 250 kilobits per second on the control and monitor buses is timed by the clock square-wave signal. The timing reference point is the falling edge of the clock signal.

Delimiter Bus. The signal on the delimiter bus is normally a logic 0, but is changed to a logic 1 during the 32-bit period that corresponds to the 32 bits of the control word (figure 10-1).

Control Bus. Data from the computer to the transmit and receive control heads consists of control words 32 bits long (numbered 0 through 31). The first
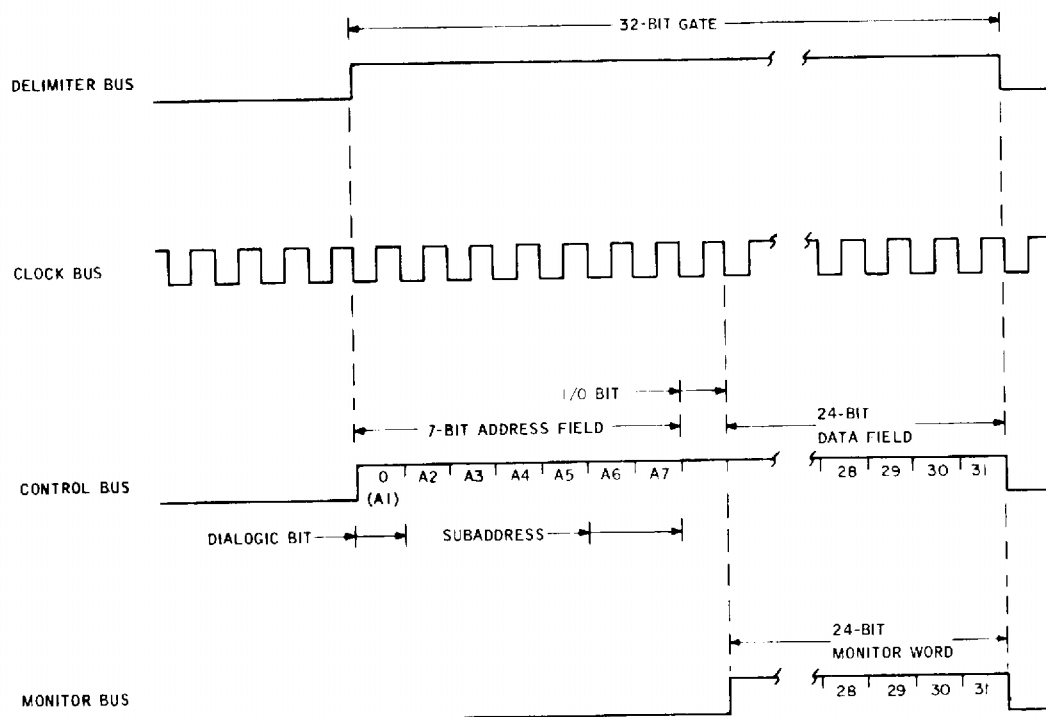

Figure 10-1. Logic Level Bus Signal Relationship

seven bits (0 through 6) make up the address field. Bit 0 is not used and is transmitted as a logic 0. The functional equipment (receiver or transmitter) and data character (frequency, mode, monitor) address are contained in bits 1 through 4 and are a programmed function of the computer. Bits 5 and 6 identify the particular radio group being serviced. Selection is made by hardwire strapping at rear connectors on the transmit and receive control heads. The data field includes bits 7 through 31. However, bit 7 is used as the input/output bit and denotes the direction of data transfer (to or from the computer). This bit is always a logic 1 when the 24-bit control word data field is examined and is a logic 0 if a monitor word is transmitted to the computer. When there is no data transferred on the control bus, a continuous logic 0 is present.

Monitor Bus. Data transferred from the transmit and receive control heads to the computer consists of three monitor words 24 bits long (numbered 8 through 31). The monitor words are transmitted from the respective control heads when the input/output bit (bit 7) of the control word is a logic 0. As shown in figure 10-1, timing of the monitor data is in-phase with the last 24 bits of the control word. The monitor bus is an open circuit when no data is being transferred.

Logic Level Monitor Word Formats. Three monitor words are transmitted on the logic level bus between each of the control heads and the computer. Table 10-3 identifies the data contained in each bit of the three receive monitor words. Receive monitor word 1 contains receiver frequency data, monitor word 2 contains receiver mode information, and monitor word 3 contains receiver squelch control information. Table 10-2 identifies the data contained in each bit of the three transmit monitor words. Transmit monitor words 1 and 2 also contain frequency and mode information, but monitor word 3 contains carrier level control information.

Logic Level Control Word Formats. One control word is transmitted on the logic level bus from the computer to the transmit control head and another control word services the receive control head. Table 10-1 identifies the data contained in each bit of these 32-bit words. The information in these control words is used primarily to light front panel indicators on the two control heads and the audio control unit.

Table 10-1

RECEIVE AND TRANSMIT LOGIC
LEVEL CONTROL WORDS

Bit No.	LLA8 Transmit Control Word	LLA4 Receive Control Word	
0	Logic 0	Logic 0	
1	Logic 1	Logic 0	
2	Logic 0 Logic Level Address Eight	Logic 1 Logic Level Address Four	
3	Logic 0	Logic 0	
4	Logic 0	Logic 0	
5	logic 0 } Radio group	logic 0 } Radio group	
6	logic 1	logic 1	
7	Logic 1 (dialogic) Always a 1	Logic 1 (dialogic)	
8	Not used	Not used	
9	Not used	Not used	
10	Not used	Not used	
11	Not used	Not used	
12	Not used	Not used	
13	Not used	Not used	
14	Not used	Not used	
15	Not used	Not used	
16	Not used	Not used	
17	Not used	Not used	
18	Not used	Not used	
19	Not used	Not used	
20	Not used	Not used	
21	Not used	Not used	
22	Not used	Not used	
23	Not used	Not used	
24	Not used	A1 channel receive audio	To audio
25	Not used	B1 channel receive audio	control
26	Not used	A2 channel receive audio	unit
27	Keyed	B2 channel receive audio	indicators
28	Self-test prove	Self-test prove	
29	Operate	Operate	
30	Frequency initiate	Frequency initiate	
31	Transmitter fault	Receive fault	

NOTE: LLA = Logic Level Address

Table 10-2

TRANSMIT LOGIC LEVEL
MONITOR WORDS

Bit No.	LLA 6 Monitor Word 1 (freq word)	LLA 7 Monitor Word 2 (mode word)	LLA 5 Monitor Word 3 (carrier level word)
8	Logic 1 *Always a 1*	Logic 1 *always a 1*	Logic 1
9	Not used	Power on	Not used
10	10 MHz (2)	Vox enable	Master/slave
11	10 MHz (1)	Simplex enable	Power interrupt
12	1 MHz (8)	B1 channel transmit	Frequency initiate
13	1 MHz (4)	Logic 0	Mode initiate
14	1 MHz (2)	A1 channel transmit	Transceiver enable
15	1 MHz (1)	Logic 0	548U enable
16	100 kHz (8)	Receive through coupler	Power level change
17	100 kHz (4)	Self-test	Servo enable
18	100 kHz (2)	B2 channel transmit	Not used
19	100 kHz (1)	CW enable	Notused
20	10 kHz (8)	AME enable	Carrier level (8)
21	10 kHz (4)	Logic 0	Carrier level (4)
22	10 kHz (2)	A2 channel transmit	Carrier level (2)
23	10 kHz (1)	Logic 0	Carrier level (1)
24	1 kHz (8)	Logic 0	Not used
25	1 kHz (4)	Logic 0	Not used
26	1 kHz (2)	Medium power	Not used
27	1 kHz (1)	Low power	Not used
28	0.1 kHz (8)	Logic 0	Not used
29	0.1 kHz (4)	Filament on	Not used
30	0.1 kHz (2)	Plate on	Not used
31	0.1 kHz (1)	Key	Not used

NOTE: Numbers in parentheses indicate weighted
BCD. LLA = Logic Level Address

Table 10-3

RECEIVE LOGIC LEVEL
MONITOR WORDS

Bit NO.	LLA 2 Monitor Word 1 (frequency)	LLA 3 Monitor Word 2 (mode)	LLA 1 Monitor Word 3 (initiate)	Bit NO.	LLA 2 Monitor Word 1 (frequency)	LLA 3 Monitor Word 2 (mode)	LLA 1 Monitor Word 3 (initiate)
8	Logic 1	Logic 1	Logic 1	20	10 kHz (8)	AME enable	Not used
9	Not used	Receiver mute	Not used	21	10 kHz (4)	B1 channel voice receive	Not used
10	10 MHz (2)	Not used	Master/slave	22	10 kHz (2)	A1 channel data receive	Not used
11	10 MHz (1)	Not used	Power interrupt	23	10 kHz (1)	A1 channel voice receive	Not used
12	1 Mhz (8)	B2 channel data receive	Frequency initiate	24	1 kHz (8)	Not used	B1 squelch (8)
13	1 MHz (4)	B2 channel voice receive	Mode initiate	25	1 kHz (4)	Not used	B1 squelch (4)
14	1 MHz (2)	A2 channel data receive	Not used	26	1 kHz (2)	Not used	B1 squelch (2)
15	1 MHz (1)	A2 channel voice receive	Not used	27	1 kHz (1)	Not used	B1 squelch (1)
16	100 kHz (8)	Not used	Not used	28	0.1 kHz (8)	Not used	A1 squelch (8)
17	100 kHz (4)	Self-test	Not used	29	0.1 kHz (4)	Power on	A1 squelch (4)
18	100 kHz (2)	B1 channel data receive	Not used	30	0.1 kHz (2)	Not used	A1 squelch (2)
19	100 kHz (1)	Not used	Not used	31	0.1 kHz (1)	Not used	A1 squelch (1)

NOTE:
1. Not used indicates bit is transmitted as logic 0.
2. Numbers in parentheses indicate weighted BCD.
3. LLA = Logic Level Address

80

NOTES