Chapter 13

TRANSMITTER TUNE CYCLE

AN/TSC-60(V1)

Transmitter Tune Cycle

Pressing the *initiate* button on the transmitter control head initiates the transmitter tune cycle. Momentary operator keying, however, is required to complete the tune cycle. When the operator presses the *initiate* button, the computer sends transmitter frequency control word 1 (and transmitter mode control words 2 and 3) to the three transmitter *DCU's* (exciter, power amplifier, and antenna coupler). This description of a tune cycle assumes an antenna coupler is used. The frequency word contains 22 bits of bcd frequency information. These bits represent the six frequency digits selected. The most significant digit (10 MHz) is a 2-bit binary-coded number, and the remaining five digits are bcd. The exciter uses all 22 bits (six digits) for frequency information; the power amplifier uses only the 10 most significant bits (three digits); and the antenna coupler uses only the 5 most significant bits (one digit and lowest even megahertz digit). Each transmitter unit *DCU/DCFE* generates a tune start pulse upon reception and recognition of the transmitter frequency control word. The tune start pulses cause the individual exciter, power amplifier, and antenna coupler *DCFE* output circuits within each unit to be set as described in the following paragraphs.

The exciter *DCFE* outputs result in the following:

a. Exciter tune output line is set to a logic 1 (tune in progress).
b. Radio key line is set to unkey.
c. Rf bandpass filter in the rf translator is coarse and fine tuned.
d. The selected operating frequency is set up by the synthesizer.
e. Monitor bit 16 is set to a logic 0 in the exciter monitor word, notifying the computer that the exciter rf tune is complete.
f. The four sideband channels are inhibited. No rf output is provided to the power amplifier during this portion of the tune cycle.

The power amplifier *DCFE* outputs result in the following:

a. Key output is set to unkey.
b. Power amplifier tune and exciter tune outputs are set to a logic 1, indicating tune in progress.
c. Power amplifier operate request and power amplifier tune complete monitor word bits 13 and 14 respectively are set to logic 0. This information is sent back to the computer, indicating power amplifier tune in progress.
d. Tune power trim resistors are placed on the power amplifier rf output.
e. The power amplifier automatic tune cycle counter is placed in the ready-to-tune position.
f. If no faults exist, all servos are enabled and the power amplifier completes band-switching and coarse tuning (power amplifier tune steps 1 and 2) without a key command.

Antenna coupler *DCFE* outputs result in the following:

a. Ground is removed from the rf key interlock to the power amplifier.
b. Antenna coupler tune complete monitor bit 12 is sent to the computer as a logic 0 in the coupler monitor word to indicate coupler tune incomplete.
c. Antenna coupler tuning elements are sent to the home (digital) position, where they remain until the transmitter is keyed.

NOTE: A hard-wire rf key interlock is diplexed on the rf cable between the antenna coupler and the power amplifier. The coupler applies a dc ground on the rf interlock to the power amplifier after the coupler receives the *CCCS* key command (a logic 1 in control word 2 bit 31) and when it is ready to receive rf power from the power amplifier (tuning elements in home position). This is used as a protective device to ensure that rf is not applied to the coupler (the power amplifier is not keyed) until the coupler is ready for it. Further coupler protection is achieved by ensuring that the *CCCS* key and unkey commands are transmitted to the equipment so that rf is not present when the key command changes. This requirement is fulfilled by sending new key data to the transmitter *DCU's* in this sequence: exciter, antenna coupler, and power amplifier. Thus, the key command is required at the antenna coupler before the power amplifier receives the key command, and rf is removed by unkeying the exciter before the antenna coupler and power amplifier receive the command to unkey.

Momentary operator keying of the transmitter is now required to further advance the tune cycle. The

computer transmits the key command to the transmitter units when the keying is energized by the operator. If key is hard-wired for normal operation, the computer examines key monitor bit 18 from the power amplifier for a logic 1 keyed indication. When the key monitor bit is a logic 1 as a result of either *CCCS* or hard-wire keying, the computer latches the key command until the tune cycle is completed.

When the transmitter is keyed, the exciter provides a -3-dB carrier (referenced to full-carrier) to the power amplifier. Ground is applied to the power amplifier rf key interlock from the antenna coupler. The power amplifier starts fine-tuning (power amplifier tune step 3) and provides rf to the antenna coupler with trim resistors on the power amplifier output. All power amplifier tuning servos are enabled except the loading servo. Tgc is applied to the exciter from the power amplifier. Tgc adjusts the overall transmitter gain during power amplifier tuning steps 3 through 5. The power amplifier continues to fine-tune, automatically progressing to power amplifier tune step 4, while the antenna coupler is fine-tuning. Fine-tuning is automatically initiated in the antenna coupler when the transmitter is keyed. Fine-tuning envolves series-resonating the antenna and translating the resonated load to less than 50 ohms. When this is accomplished, the fine-tune cycle is complete and a second fine-tune is enabled. Resonating and loading adjustments are accomplished automatically during the second fine-tune cycle in the antenna coupler. The power amplifier rf output is approximately 200 watts at the end of power amplifier tune step 4. As soon as the reflected power falls below the specified level in the second fine-tune cycle, the antenna coupler places a logic 1 in its monitor word bit 12 position. This is an indication to the computer that the antenna coupler has completed its analog-tune cycle and is ready for normal operating input power levels. The computer receives this antenna coupler tune complete indication, and transmits a logic 0 in power amplifier tune bit 28 of transmitter control word 2. In response to the logic 0 in power amplifier tune bit 28, the power amplifier advances the power amplifier tune cycle to step 5 and removes the trim resistors in the power amplifier output. All power amplifier servos are enabled during this tune step for a final tune cycle trim adjustment. The power amplifier completes final tune step 5 and places a logic 1 in power amplifier operate request bit 13 of the power amplifier monitor word. This information is sent to the computer, signifying that the power amplifier is ready to return to normal operation. The transmitter output power at this time is adjusted to 500 watts by tgc action (with *HIGH* power mode selected). The exciter tgc circuits now stabilize, and the exciter sends a logic 0 in tgc monitor bit 15 of the exciter monitor word to the computer. When the computer receives the logic 1 power amplifier operate request bit and the logic 0 exciter tgc monitor bit, it transmits a logic 0 in exciter tune bit 25 of control word 2. A logic 0 in the exciter tune bit causes the exciter *DCFE* to remove the -3-dB carrier and to enable the four sideband channels. Rf drive is removed from the power amplifier, and the exciter is returned to normal operation. Exciter tune logic 0 causes the power amplifier *DCFE* to turn off all power amplifier servos and return the power amplifier to normal operation. As a result, the power amplifier sends power amplifier tune complete logic 1 and power amplifier operate request logic 0 to the computer. Exciter tune logic 0 turns off the antenna coupler servos, ending the coupler tune cycle. Power amplifier tune complete logic 1 from the power amplifier notifies the computer that the power amplifier has returned to the normal operating condition (tune step 6), and that the key command should be unlatched and returned to operator control. The *OPR* lamp lights when the computer receives the logic 1 power amplifier tune complete bit, notifying the operator that the transmitter tune cycle is complete.

AN/TSC-60(V2)

Automatic Tuning

Circuit breakers must first be *ON* to energize equipment. When a command is received to turn on the power amplifier filaments, the control logic activates the blower (if the access/plug interlock circuit is complete). When the air sensor returns a signal indicating that adequate air is being supplied by the blower, the filaments are enabled and a filament timer is turned on. The timer prevents enabling the high voltage until the filaments have been on for approximately 30 seconds. The filament timer is bidirectional and if the filaments have been off for a relatively short period, the turn-on delay will be correspondingly shortened. The high-voltage enable command may be received at any time. When the filaments have been off, the control logic will cause the power amplifier to go through a tune cycle. After the high voltage has been enabled and the high-voltage monitor indicates that high voltage is present, the control logic will be released to begin a tune cycle.

The tuning sequence consists of the following seven steps:

Step 1 - Ready to Tune

Tune start is initiated by a new type I (frequency) control word. The sequence counter is set to step 1 and a course tuning frequency analog is developed. All four tuning servos are disabled and the equipment remains in step 1 until high voltage is present and all faults and interlocks are satisfied.

Step 2 - Coarse Tune

When the conditions of step 1 have been satisfied, coarse tuning may be initiated by a key enable or auxiliary key enable signal. The sequence counter advances to step 2, all four tuning servos are enabled, and the amplifier is course tuned. Step 2 is held until the servos have nulled (indicated by the servo run sensor signals) and RF output from the exciter is present (indicated by the RF input sensor signal). All faults and interlocks must remain satisfied and the transmitter must remain keyed. (Key monitor signal indicates key enable status.)

Step 3 - Fine Tune 1

Fine tuning is initiated automatically when step 2 conditions are satisfied. The sequence counter advances to step 3, the loading servo is disabled, and the servo mode relay switches from coarse to fine tune inputs. The ALC/TGC relay control selects TGC and the tune power control selects the tuning power level. The power amplifier key line keys the transmitter. Step 3 is held until the servos are nulled and RF is present on the plate of the power amplifier (indicated by the RF prove signal). The fault, interlock, and RF input sensor signals must remain normal and the transmitter must remain keyed.

Step 4- Fine Tune 2

When step 3 conditions are satisfied, tuning proceeds automatically to step 4. Step 4 continues the conditions of step 3 except that the loading servo is also enabled. Step 4 is held until all four tuning servos null.

Step 5 - Fine Tune 3

When the conditions of steps 3 and 4 are satisfied, tuning proceeds automatically to step 5. Step 5 continues the conditions of steps 3 and 4 until the power amplifier tune signal indicates the associated antenna coupler has tuned. In the absence of an antenna coupler, the pa tune signal is controlled by the exciter.

Step 6 - Full Power Trim

When the pa tune signal indicates that associated equipment is tuned, the tune sequence counter advances to step 6 and the tune power control signals enables full power operation of the power amplifier. The power amplifier is still protected against overload by TGC. Step 6 is held until the servos have completed any final trimming necessary and the exciter tune/operate signal indicates that the exciter has finished tuning.

Step 7 - Operate

When tuning is complete, the tune sequence counter advances to step 7, the servos are disabled, and the ALC/TGC relay control selects ALC. The pa operate request and tune complete signals indicate the power amplifier is tuned and ready to operate.

The tune sequence must be completed in 20 seconds or less or a tune fault signal will be generated.

Table 13-1

AN/TSC-60 (V2) POWER AMPLIFIER

MONITOR WORDS

BIT NO.	MONITOR WORD 1 (DIGITAL)	MONITOR WORD 2 (ANALOG)
0	Dialogic bit (0)	Dialogic bit (0)
1		
2		
3	DCU address	DCU address
4		
5		
6	DCFE subaddress	DCFE subaddress
7	DCFE subaddress	DCFE subaddress
8	Parity	Parity
9	Power interrupt	Power interrupt
10	Power fault summary	Power fault summary
11	Tune fault summary	Tune fault summary
12	Zero (0)	Filament timer
13	Pa operate request	ADC complete
14	Pa tune complete	ADC sign
15	Zero (0)	ADC overrange (100)
16	Tune fault	ADC output (80)
17	Reflected power fault	ADC output (40)
18	Key monitor	ADC output (20)
19	Pa plate current fault	ADC output (10)
20	Pa screen current fault	ADC output (8)
21	RF input monitor	ADC output (4)
22	Access/plug interlock fault	ADC output (2)
23	Circuit breakr fault	ADC output (1)
24	Antenna interlock fault	ADC output (0.8)
25	Regulator monitor	ADC output (0.4)
26	Blower transfer monitor	ADC output (0.2)
27	Servo error 2	ADC output (0.1)
28	Servo error 1	Not used
29	Counter out A	Not used
30	Counter out B	Not used
31	Counter out C	Not used

Table 13-2

CONTROL WORDS

BIT NO.	TYPE I (FREQUENCY)	TYPE II (MODE)	TYPE III (MULTIPLEX ADDRESS)	TYPE IV (DIGITAL MON REQ/MAINT)
0	Dialogic bit (1)	Dialogic bit (1)	Dialogic bit (1)	Dialogic bit (1)
1	DCU address	DCU address	DCU address	DCU address
2				
3				
4				
5				
6	DCFE subaddress 0	DCFE subaddress 0	DCFE subaddress 1	DCFE subaddress 1
7	DCFE subaddress 0	DCFE subaddress 1	DCFE subaddress 0	DCFE subaddress 1
8	Parity	Parity	Parity	Parity
9	Not used	Not used	Not used	Error monitor request
10	10 MHz 2 (MSD)	Not used	ADC inhibit	Auto/manual tune
11	10 MHz 1 (LSD)	Not used	ADC mux address 16	Servo activate
12	1 MHz 8 (MSD)	Not used	ADC mux address 8	Not used
13	1 MHz 4	Not used	ADC mux address 4	Not used
14	1 MHz 2	Not used	ADC mux address 2	Not used
15	1 MHz 1 (LSD)	Not used	ADC mux address 1	Not used
16	100 kHz 8 (MSD)	Not used	Not used	Not used
17	100 kHz 4	Not used	Not used	Not used
18	100 kHz 2	Not used	Not used	Not used
19	100 kHz 1 (LSD)	Not used	Not used	Not used
20	10 kHz 8 (MSD)	Not used	Not used	Servo 4 disable
21	10 kHz 4	Not used	Not used	Servo 3 disable
22	10 kHz 2	Not used	Not used	Servo 2 disable
23	10 kHz 1 (LSD)	Not used	Not used	Servo 1 disable
24	Not used	Auxiliary function	Not used	Servo 4 mode
25	Not used	Exciter tune	Not used	Servo 3 mode
26	Not used	Medium power	Not used	Servo 2 mode
27	Not used	Low power	Not used	Servo 1 mode
28	Not used	Pa tune	Not used	Control A
29	Not used	Power on/filament on	Not used	Control B
30	Not used	Plate on	Not used	Control C
31	Not used	Key	Not used	Servo enable

Table 13-3

309F-1: AUTOMATIC TUNING SEQUENCE, LOGIC SUMMARY

STEP	MODE	SEQUENCE COUNTER			$\overline{\text{SERVO ENABLE}}$				SERVO MODE CONTROL				$\overline{\text{PA OPERATE RQST}}$	$\overline{\text{ALC}}$/TGC RELAY CONT	PA KEY LINE	TUNE COMPLETE	TUNE PWR CONT	TUNE SEQ POS (BIT A)	TUNE SEQ POS (BIT B)	TUNE SEQ POS (BIT C)
		U19	U20	U21	DRIVER	PRIMARY	SECONDARY	LOADING	DRIVER	PRIMARY	SECONDARY	LOADING								
		A	B	C																
1	Ready to tune	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0
2	Coarse tune	1	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0
3	Fine tune 1	0	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	1	0
4	Fine tune 2	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1
5	Fine tune 3	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1
6	Full power trim	1	0	1	0	0	0	0	0	0	0	0	1/0	1	1	1	0	1	0	1
7	Operate	1	1	1	1	1	1	1	0	0	0	0	1	0	1/0	0	0	1	1	1

Table 13-4

309F-1: MANUAL TUNING SEQUENCE, LOGIC SUMMARY

STEP	MODE	$\overline{\text{CONT A}}$	$\overline{\text{CONT B}}$	$\overline{\text{CONT C}}$	SEQUENCE COUNTER			$\overline{\text{SERVO DISABLE}}$				$\overline{\text{SERVO ENABLE}}$			
					U19	U20	U21	DRIVER	PRIMARY	SECONDARY	LOADING	DRIVER	PRIMARY	SECONDARY	LOADING
					A	B	C								
1	Ready to tune	0	1	1	1	0	0					1	1	1	1
2	Coarse tune	0	0	1	1	1	0	1/0	1/0	1/0	1/0	0/1	0/1	0/1	0/1
3	Fine tune 1	1	0	1	0	1	0	1/0	1/0	1/0		0/1	0/1	0/1	1
4	Fine tune 2	1	0	0	0	1	1	1/0	1/0	1/0	1/0	0/1	0/1	0/1	0/1
5	Fine tune 3	1	1	0	0	0	1	1/0	1/0	1/0	1/0	0/1	0/1	0/1	0/1
6	Full power trim	0	1	0	1	0	1	1/0	1/0	1/0	1/0	0/1	0/1	0/1	0/1
7	Operate	0	0	0	1	1	1					1	1	1	1

Table 13-5

309F-1: SUMMARY OF DIGITAL-TO-ANALOG CONVERTER CODES

TX/RX FREQUENCY (MHz)	SHIFT REGISTER																LADDER R-NETWORK											
	10 MHz BITS		1 MHz BITS				100 kHz BITS				10 kHz BITS				10 MHz BIT WT		1 MHz BIT WT				100 kHz BIT WT				10 kHz BIT WT			
	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	1	2	4	2	1	2	4	2	1	2	4	2	1
02.00XX	1	1	1	1	0	1	1	1	1	1	1	1	1	1					X									
02.01XX	1	1	1	1	0	1	1	1	1	1	1	1	1	0					X									X
02.02XX	1	1	1	1	0	1	1	1	1	1	1	1	0	1					X								X	
02.03XX	1	1	1	1	0	1	1	1	1	1	1	1	0	0					X								X	X
02.04XX	1	1	1	1	0	1	1	1	1	1	1	0	1	1					X							X		
02.05XX	1	1	1	1	0	1	1	1	1	1	1	0	1	0					X							X		X
02.06XX	1	1	1	1	0	1	1	1	1	1	1	0	0	1					X							X	X	
02.07XX	1	1	1	1	0	1	1	1	1	1	1	0	0	0					X							X	X	X
02.08XX	1	1	1	1	0	1	1	1	1	1	0	*0	*0	1					X						X	X	X	
02.09XX	1	1	1	1	0	1	1	1	1	1	0	*0	*0	0					X						X	X	X	X
02.10XX	1	1	1	1	0	1	1	1	1	0	1	1	1	1					X					X				
02.20XX	1	1	1	1	0	1	1	1	0	1									X				X					
02.30XX	1	1	1	1	0	1	1	1	0	0	1	1	1	1					X				X	X				
02.40XX	1	1	1	1	0	1	1	0	1	1	1	1	1	1					X			X						
02.50XX	1	1	1	1	0	1	1	0	1	0	1	1	1	1					X			X		X				
02.60XX	1	1	1	1	0	1	1	0	0	1	1	1	1	1					X			X	X					
02.70XX	1	1	1	1	0	1	1	0	0	0	1	1	1	1					X			X	X	X				
02.80XX	1	1	1	1	0	1	0	*0	*0	1	1	1	1	1					X		X	X	X					
02.90XX	1	1	1	1	0	1	0	*0	*0	0	1	1	1	1					X		X	X	X	X				
02.99XX	1	1	1	1	0	1	0	*0	*0	0	0	*0	*0	0					X		X	X	X	X	X	X	X	X
03.00XX	1	1	1	1	0	0	1	1	1	1	1	1	1	1					X	X								
04.00XX	1	1	1	0	1	1	1	1	1	1	1	1	1	1				X										
05.00XX	1	1	1	0	1	0	1	1	1	1	1	1	1	1				X		X								
06.00XX	1	1	1	0	0	1	1	1	1	1	1	1	1	1				X	X									
07.00XX	1	1	1	0	0	0	1	1	1	1	1	1	1	1				X	X	X								
08.00XX	1	1	0	*0	*0	1	1	1	1	1	1	1	1	1			X	X	X									
09.99XX	1	1	0	*0	*0	0	0	*0	*0	0	0	*0	*0	0			X	X	X	X	X	X	X	X	X	X	X	X
10.00XX	1	0	1	1	1	1	1	1	1	1	1	1	1	1		X												
19.99XX	1	0	0	*0	*0	0	0	*0	*0	0	0	*0	*0	0		X	X	X	X	X	X	X	X	X	X	X	X	X
20.00XX	0	*0	1	1	1	1	1	1	1	1	1	1	1	1	X	X												
29.99XX	0	*0	0	*0	*0	0	0	*0	*0	0	0	*0	*0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X Indicates weight selected by shift register outputs
*Indicates diode decoding

NOTES