Chapter 6

LOGIC GENERATORS AND ASSOCIATED CIRCUITS

INTRODUCTION

There are two general classes of oscillators: *sinusoidal* and *relaxation.* Sinusoidal oscillators generate sine waves. Relaxation oscillators generate nonsinusoidal waveforms. The name *relaxation* is used because these oscillators are characterized by a sudden change or relaxation from one state of equilibrium to another. The line of demarcation between the two types is not always sharply defined.

A multivibrator is a type of relaxation oscillator employing a two-stage amplifier, with the the output of the second stage regeneratively coupled to the input of the first stage and with the output of the first regeneratively coupled to the input of the second stage. The output of a multivibrator is usually a rectangular waveshape.

There are three general types of multivibrators: the *astable* multivibrator; the *monostable multivibrator, and the bistable* multivibrator. The monostable and bistable find the moxt extensive use in computers.

The astable multivihbrator (also called the *free-running* multivibrator) produces a continuous square wave or rectangular wave as long as power is applied to the circuit.

The bistable multivibrator is also called the *Eccles-Jordan* or *flip flop.* It produces half of an output cycle with one input trigger. Two triggers are necessary to produce a complete cycle. This multivibrator is the basic building block for the logic generator or logic flip flop.

The monostable multivibrator is also called the *one-shot* multivibrator and is used in computers for pulse stretching, pulse shaping, operating gates, and for providing adjustable delayed gates. This multivibrator is also capable of producing several different output.

INFORMATION

TRANSISTOR BISTABLE (ECCLES-JORDAN) MULTIVIBRATOR

A basic bistable multivibrator and its waveforms are shown in figures 6-1 and 6-2. In the stable state, one transistor is conducting while the other is cut off. The states are switched with the proper application of a trigger pulse.

Referring to figure 6-1, R1 and R2 are collector load resistors; R1, R3, and R7 form the voltage dividing network to develop forward bias for Q2. R2, R4, and R5 form the voltage dividing network to develop forward bias for Q1.

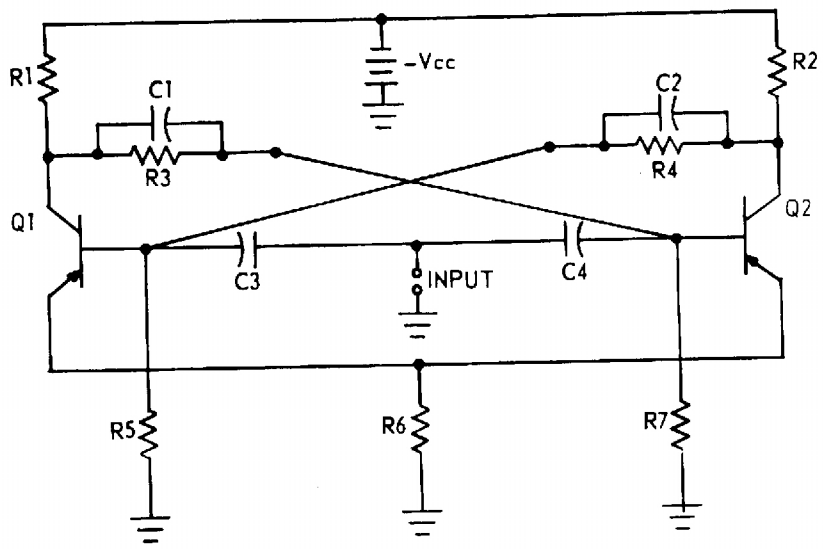

Figure 6-1. Bistable MV

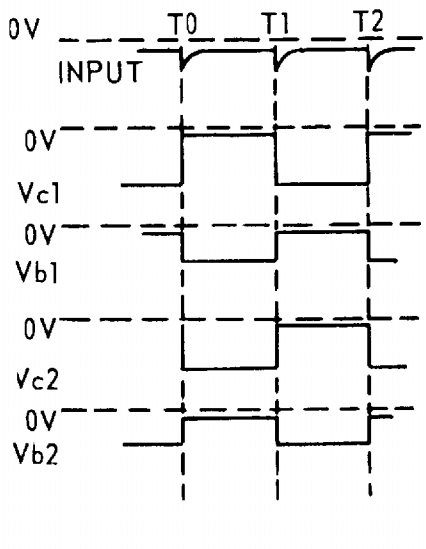

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Figure 6-2. Waveshapes

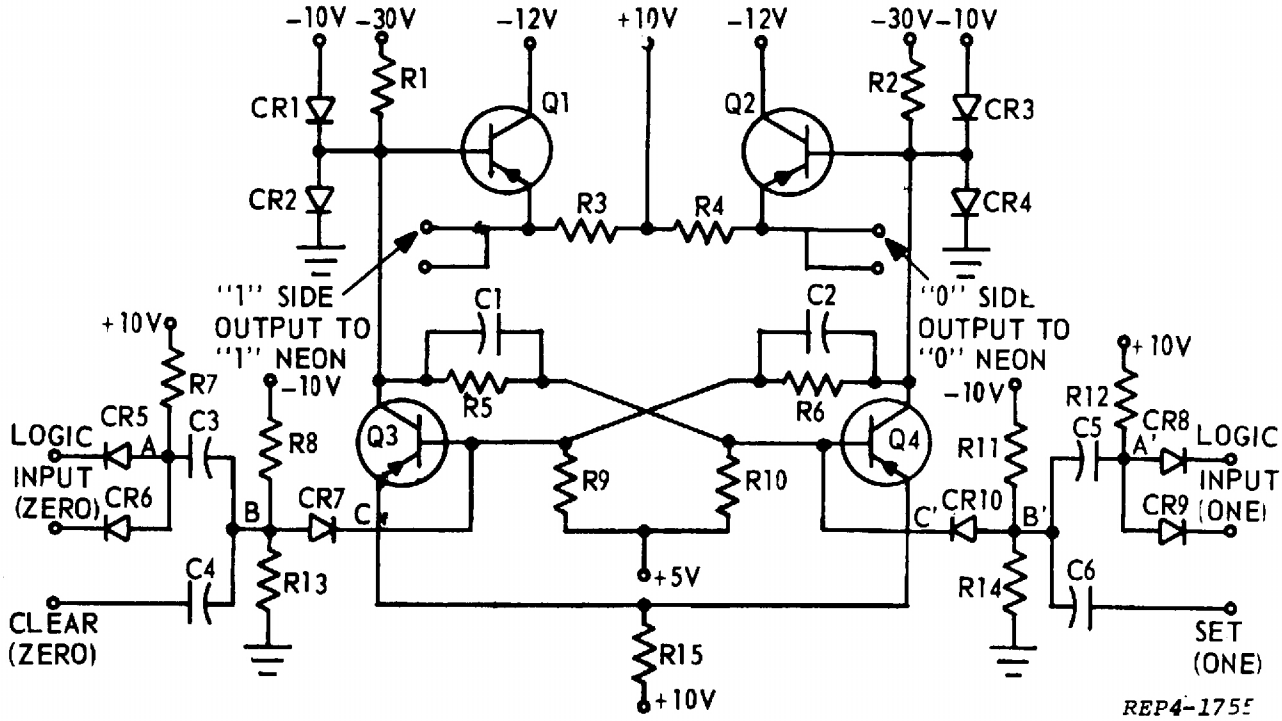

Figure 6-3. Flip Flop With AND Gates

C1 and C2 couple fast changes to increase switching action.

Assume that prior to T1, Q1 is cut off, the collector voltage (Vc1) is at a negative Vcc, and the base voltage (Vb1) is near zero volts; the base voltage (Vb2) is negative. At T0 a trigger is applied to the input. This negative trigger is coupled through C3 and C4 to the bases of Q1 and Q2. Q2 is conducting so the trigger has no effect on the conduction of Q2. Q1 is cut off and the negative trigger increases the forward bias to a point where it conducts.

Vc1 then goes from a negative Vcc to slightly less than zero volts; this causes the base voltage of Q2 to go towards zero volts and cut off. Vc2 then goes toward a negative Vcc. This negative voltage is coupled over to the base of Q1 and keeps Q1 conducting. Thus, a stable state of Q1 conducting and Q2 cut off is reached.

The flip flop will remain this way until another negative trigger is received at T1. This negative trigger is coupled through C3 and C4 to the base of Q1 and Q2. Q2 is conducting so the trigger has no effect on the conduction of Q2. Q1 is the cutoff and the negative ttrigger increases the forward bias to a point where it conducts Vc1, then goes from a negative Vcc to slightly less than zero volts; this causes the base voltage of Q2 to go towards zero volts and cutoff. Vc2 then goes toward a negative Vcc. This negative voltage is coupled over to the base of Q1 and keeps Q1 conducting.

Thus, a stable state of Q1 conducting and Q2 cut off is reached. The flip flop will remain this way until another negative trigger is received at T2.

TRANSISTOR LOGIC FLIP-FLOP WITH GATE INPUTS FOR UP-CLOCK OPERATION

In figure 6-3 is the schematic for a transistor logic flip flops with modifications for use in logic circuits.

The following is the circuit analysis of the flip flop. Q1 and Q2 are emitter followers and the outputs are taken from their emitters. CR1, CR2, CR3, and CR4 are clamping diodes that maintain the logic levels at zero and -10 volts.

Q3 and Q4 form the actual multivibrator. Q3 is the one-side transistor and Q4 is the zero-side transistor. R1 and R2 are collector load resistors; R2, R6, and R9 form the voltage dividing network for forward bias of Q3. R1, R5, and R10 form the voltage dividing network for forward bias for Q4. The forward bias is being developed across R9 and R10. C1 and C2 couple fast changes to increase the flip flop speed.

The inputs to the flip flop consist of a set and reset input and two input AND gates. CR5, CR6, and R7 form the AND gate that feeds the one-side transistor and clocks the flip flop to the zero state. CR8, CR9, and R12 form the AND gate that feeds the zero side transistor, clocks the flip flop to the one state. C3, R13, and C5 and C14 are differentiating networks that differentiate the outputs of the AND gates. C4, R13, and C6 and R14 form differentiating networks for the set and reset inputs; the reset input is fed to C4 and the set input is fed to C6. R8, R13, and R11 and R14 form voltage dividing networks that place a negative potential on the anodes of CR7 and CR10.

This negative potential allows CR7 and CR10 to conduct only on the positive spike of the differentiated wave and permits CR7 and CR10 to perform their functions as limiting diodes, clipping the negative spikes. The outputs to the clock neons are used to ionize neon indicators so that the state (one or zero) of the flip flop can be determined by visual inspection.

In carrying this logic flip flop through a cycle of operation, refer to figures 6-3 and 6-4.

At T0 the flip flop is in the one state. This means Q3 is conducting and Q4 is cut off. The one side output is at zero volts and the zero side output is at -10 volts (figure 6-4). At T1, signals are applied to CR5, CR6, CR8, and CR9. In this case the same inputs that are applied to CR5 and CR6 are applied to CR8 and CR9 (figure 6-4).

The signals, A, B, C, A', B', and C', in figure 6-4 are the signals found at points A, B, C, A', B', and C', in figure 6-3. The signals A and A' are the outputs of the corresponding AND gates. The signals B and B' are the outputs of the corresponding differentiating networks. C and C' are the outputs of the corresponding limiting diodes. Since both input circuits and their waveshapes are the same, it is sufficient to explain only one input circut. The input signals to the circuit consisting of CR5, CR6, R7, R8, R13, and CR7 are both high only from T1 to T2 and T5 to T6. This is the only time an output will be present as illustrated by signal A in figure 6-4.

Signal A is then differentiated by C3 and R13 (signal B) and the negative spike is clipped off by CR7; the resulting waveshape is signal C. The operation of the zero side inptu circuit is the same. Only the numbers have been changed. The positive spike of signals C and C' are applied simultaneously to the bases of Q3 and Q4. At T1 the positive spike applied to the base of Q4 will have no effect because Q4 is already cut off. The positive spike applied to the

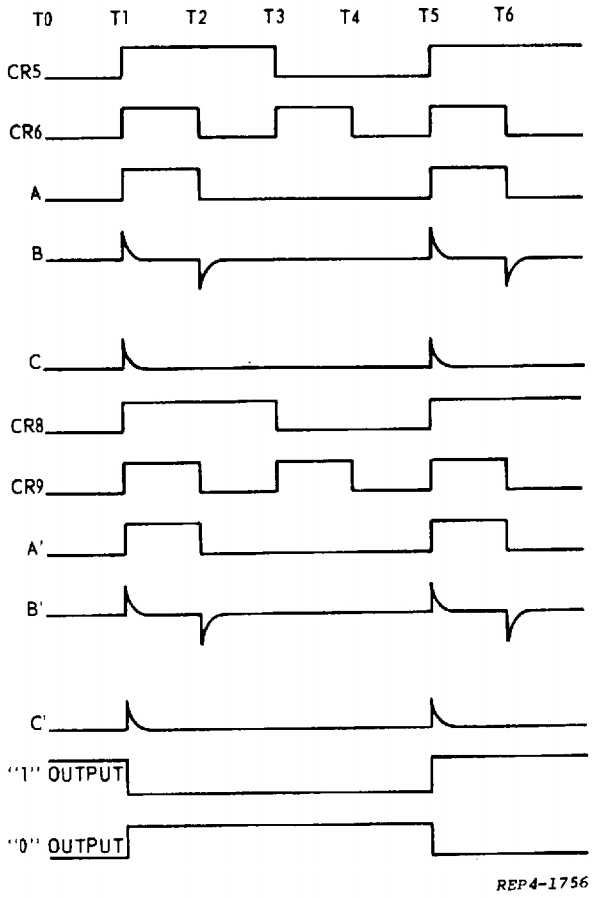

Figure 6-4. Waveforms

base of Q3, however, will cut off Q3. When the collector voltage goes negative, this negative change is coupled by C1 to the base of Q4 and Q4 goes into conduction. Q4 collector potential decreases toward zero volts. This decrease is coupled by C2 to the base of Q3 and keeps Q3 cut off.

Immediately after T1, Q3 is cut off and the collector voltage is at a -10 volts because of the logic level establishing diode CR1. This low is applied to the base of Q1 and off the emitter of Q1, a -10V is taken. This is the one side output.

Immediately after T1, Q4 is saturated and the collector is zero volts because of CR4. This high is applied to the base of Q2 and off the emitter of Q2, zero volts is taken. This is the zero side output.

The flip flop remains in this stable state, the zero state, until T5, when anothrer positive trigger is applied to the bases of Q3 and Q4. At this time the positive trigger will cut Q4 off and clock the flip flop to the one state with Q3 conducting and Q4 cut off.

In summarizing, notice that:

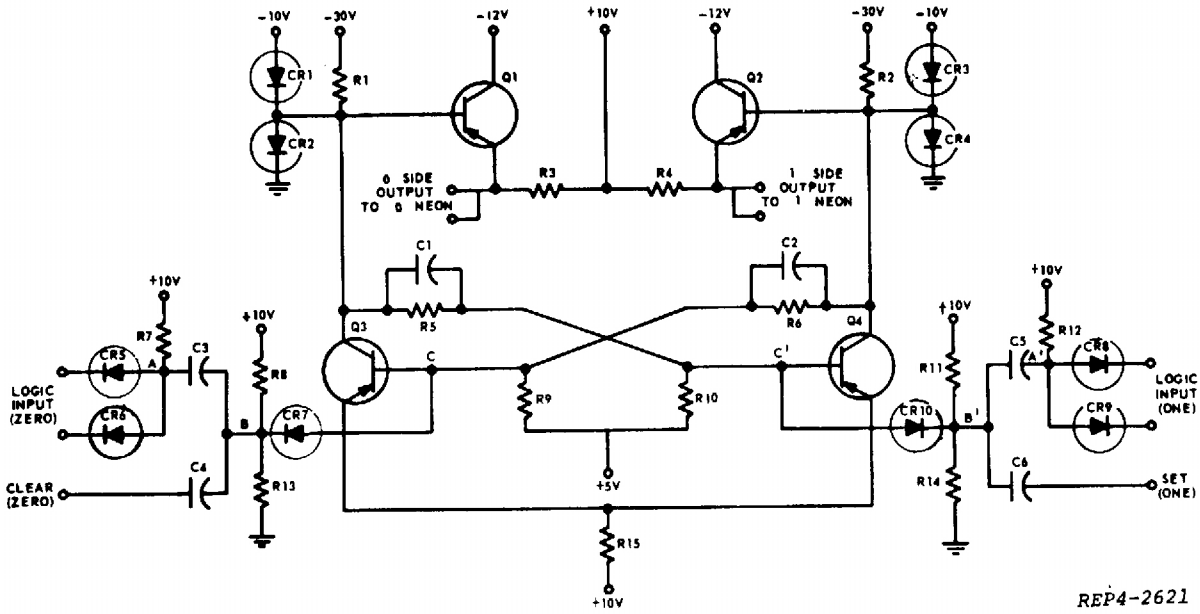

Figure 6-5. Logic Flip Flop

1. Q3 is the one side transistor.

2. Q4 is the zero side transistor.

3. In the one state, Q3 is conducting; Q4 is cut off.

4. In the zero state, Q4 is conducting and Q3 is cut off.

5. If the flip flop is in the one state, a positive trigger is applied to Q3 to clock it to the zero state.

6. If the flip flop is in the zero state, a positive trigger is applied to Q4 to clock it to the one state.

7. It changes states on the up clock of the input signal.

TRANSISTOR LOGIC FLIP FLOP WITH AND-GATE INPUTS FOR DOWN CLOCK OPERATION

Figure 6-5 is the schematic of a logic flip flop with AND gate inputs. This flip flop is basically an Eccles-Jordan multivibrator with modifications for use in logic circuits.

The following is the circuit analysis of this type of flip flop: Q1 and Q2 are emitter followers for the output, and CR1, CR2, CR3, and CR4 are limiting diodes that maintain the logic levels at zero and -10 volts. The output from Q1 and Q2 may be used to ionize neon indicators to show the state of the flip flop by visual inspection.

Q3 and Q4 form the actual multivibrator. Q3 is the zero side transistor and Q4 is the one side transistor. R1 and R3 are collector load resistors. R2, R6, and R9 form the voltage divider network for biasing Q3. R1, R5, and R10 form the voltage divider network for biasing Q4. C1 and C2 couple fast changes to increase flip flop switching speed.

The inputs to the flip flop consist of *SET* (one) and CLEAR (zero), both of which bypass the *logic input* AND gates. CR5, CR6, and R7 form the AND gate that feeds the zero side transistor and changes the flip flop to the zero state. CR8, CR9, and R12 form the AND gate that feeds the one side transistor and changes the flip flop to the one state. C3-R13 and C5-R14 differentiate the outputs of the AND gates. C4-R13 and C6-R14 differentiate the *CLEAR* and *SET* inputs. R8-R13 and R11-R14 form voltage divider networks that place a positive potential on the cathodes of CR7 and CR10. This positive potential holds CR7 and CR10 cut off until the negative spike of the differentiated wave is applied. CR7 and CR10 perform the function of a limiter diode, clipping the positive spike. CR7 and CR10 are called *clipping* diodes.

While we trace this logic flip flop through a cycle of operation, refer to both figures 6-5 and 6-6.

At T0, the flip flop is in the one state; Q4 conducting and Q3 cut off. The one output is zero volts and the zero output is -10 volts. CR1 and CR3

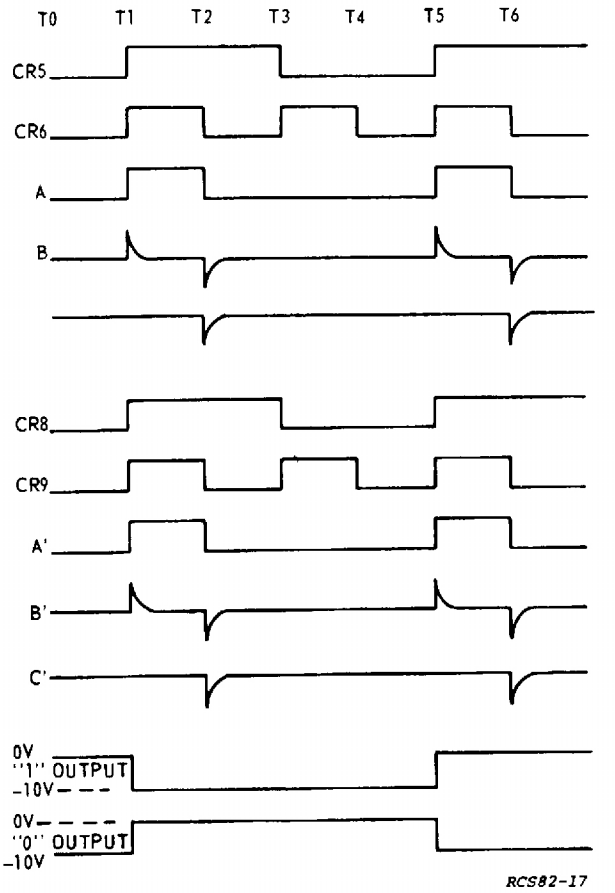

Figure 6-6. Logic Flip Flop Waveshapes

are called *clamping* diodes; they clamp the negative outputs at -10 volts.

At T1, signals are fed to CR5, CR6, CR8, and CR9 as shown by the waveforms of figure 6-6 output of AND circuit CR5-CR6 will be high (both diodes open) only when both inputs are high. The voltage at point A is +10 volts; this is shown as waveform A. This signal is differentiated by C3 and R13 and appears as waveform B across R13. The positive spike is eliminated from waveform B by limiter diode CR7, and negative trigger (waveform C) appears on the base of Q3. The same thing is happening to the inputs applied to CR8 and CR9. This is shown by waveforms A', B', and C'. The negative trigger which appears on the base of Q4 will have no effect because Q4 is already saturated. The negative trigger applied to Q3 makes it conduct, and the collector potential of Q3 goes to zero volts. This change is coupled to the base of Q4 and turns Q4 off, making the colector voltage to -10 volts. This negative going change is coupled to the base of Q3 and keeps it conducting. At T2, therefore, the one output will be at -10 volts and the zero output will be at zero volts. The flip flop is in zero state until the next trigger is applied to Q3 and Q4 at T6. At time T6 the negative trigger will turn Q4 on and cut Q3 off, which returns the flip flop to the one state.

In summary, notice that:

1. Q3 is the zero side transistor.
2. Q4 is the one side transistor.
3. In the one state, Q3 is cut off; and Q4 is conducting.
4. In the zero state, Q3 is conducting; and Q4 is cut off.
5. If the flip flop is in the one state, the negative trigger applied to Q3 will change the flip flop to the zero state.
6. If the flip flop is in the zero state, the negative trigger applied to Q4 will change the flip flop to the one state.

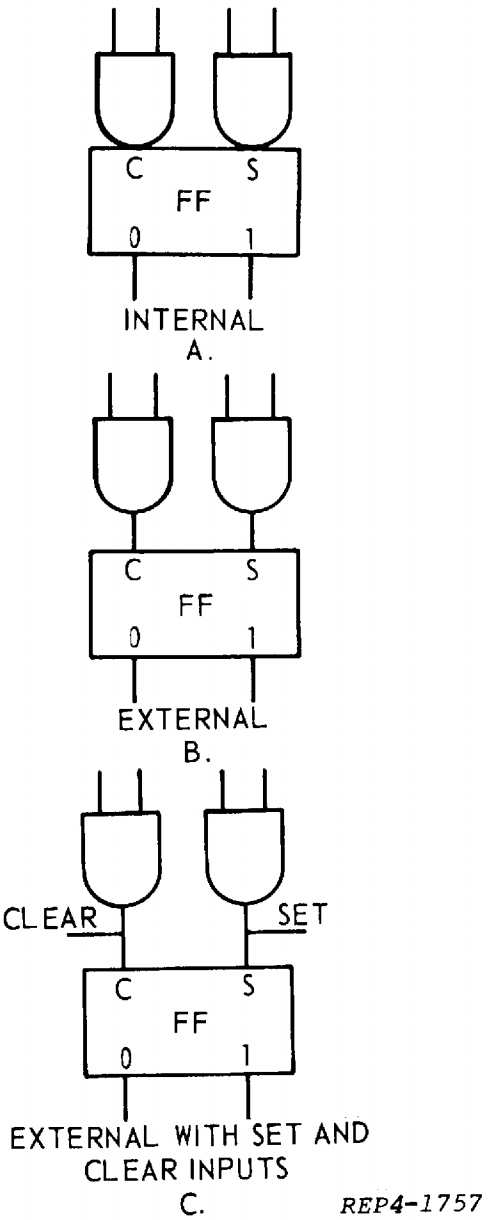

Figure 6-7. Logic Symbols for Flip Flop Waveshapes

7. The flip flop changes state on the down clock (negative going edge) of the input signal.

The logic symbol in figure 6-7A is used when the logic AND gates are integral with the flip flop. The logic symbol in figure 6-7B is used when the logic gates are separate from the flip flop. The logic symbol of figure 6-7C fits the schematic of the flip flop of figure 6-5 if the AND gates are external.

SCHMITT TRIGGER

If the waveshape of a square wave signal becomes distorted or rounded, a Schmitt trigger circuit may be used. This circuit will furnish a sharp rectangular output pulse of about the same duration and polarity as the input signal. The Schmitt trigger restores a distorted square wave to its original shape.

The Schmitt trigger is basically a multivibrator. The main difference is that one of the coupling networks is replaced by a common emitter resistor, providing additional regenerative feedback to obtain a faster switching time. The circuit is shown in figure 6-8.

In the quiescent state, Q1 is cut off, and Q2 is held at saturation by the negative voltage developed by the voltage dividing network R3, R4, and R5. The current through Q2 causes a voltage drop across R7, reverse biasing Q1 and keeping it cut off. The output takens from the collector of Q2 is about zero volts.

At T0, the negative signal applied to input A has sufficient amplitude to turn Q1 on. The collector of Q1 goes to about zero volts as the transistor conducts. This change in a positive direction is coupled to the base of Q2, causing a decrease in conduction. The decrease in conjunction of Q2 further increases forward bias on Q1 until it saturates. With Q1 saturated, Q2 will be cut off and the output will be close to Vcc.

The circuit remains in this state until T1 when the input voltage becomes less negative. At this time, Q1 will start to conduct less and its collector voltage begins to change in a negative direction. This change is coupled to the base of Q2 which, in turn, reflects reverse bias on Q1 to cut it off. With the collector of Q1 at negative Vcc, Q2 conducts near saturation, and the output is near zero volts.

Notice how the rounded input wave is converted to a square wave output. The sharp rise and fall of the edges is due to the regenerative feedback between Q2 and Q1. Any slght change in the conduction of Q1 is applied to the base of Q2 which changes the emitter voltage of Q1. Capacitor C1 speeds the transition from one state to the other.

Schmitt trigger circuits are not only used for squaring circuit but also as voltage level sensing circuits. Voltage sensing circuits are useful in warning or control circuitry. If the input voltage rises above or falls below a specified level, the Schmitt circuit produces an output, which activates a warning device.

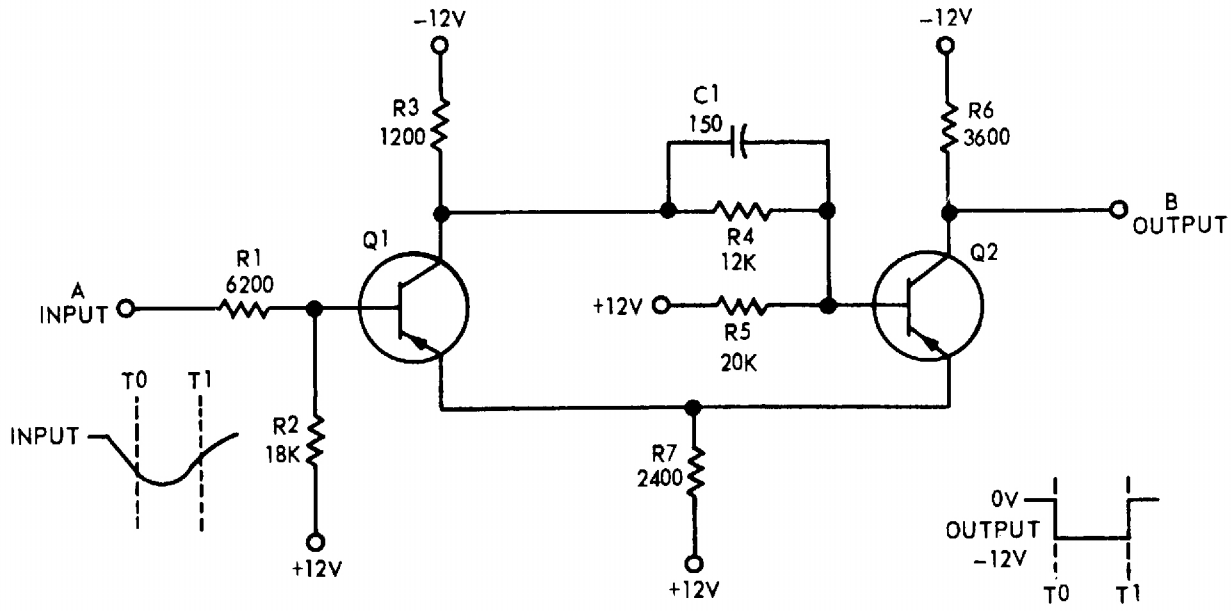

Figure 6-8. Schmitt Trigger

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LOGIC SYMBOLS

Because some circuits are used so often in digital equipment, it is an advantage to represent them by symbols (as in the case of AND, OR, NAND, and NOR circuits).

The basic bistable (Eccles-Jordan) multivibrator is modified for use in digital equipment. The modified version is called a *flip flop (FF)* and is represented by the logic symbol shown in figure 6-9.

The FF is a device which stores a single bit of information. It has three possible inputs: set (S), clear or reset (C), and toggle or trigger (T); and two possible outputs: one and zero. The S input is near the one output and the C is near the zero output. When not used, the trigger input, T, may be omitted from the symbol.

The two outputs are normally of opposite polarity. A one is stored in the FF when the one output level is active (high) and the zero output level is inactive (low). A zero is stored in the FF when the above condition is reversed.

The FF assumes the one state when a signal appears at the S input regardless of the original state. It assumes the zero state when a signal appears at the C input regardless of the original state. It reverses its state when a signal appears at the T input. There are several possible variations to normal FF operations when inputs are applied to more than one input simultaneously.

A modified version of the monostable multivibrator is the single shot (SS). The symbols are shown in figure 6-10. Output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the SS and not by the input signal. Waveforms may be shown inside or outside the symbol. The unactuated state of the SS is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state for the duration of the active time of the SS (pulsewidth) or 0.5 microsec in figure 6-10.

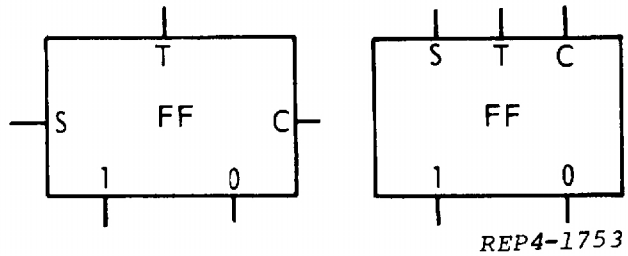

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Figure 6-9. Flip Flop Multivibrator Symbol

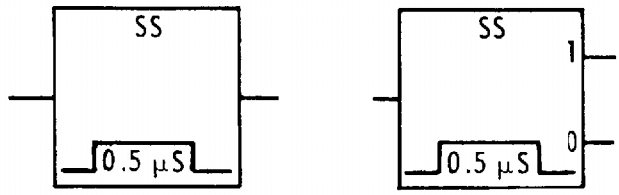

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Figure 6-10. Single Shot Multivibrator Symbols

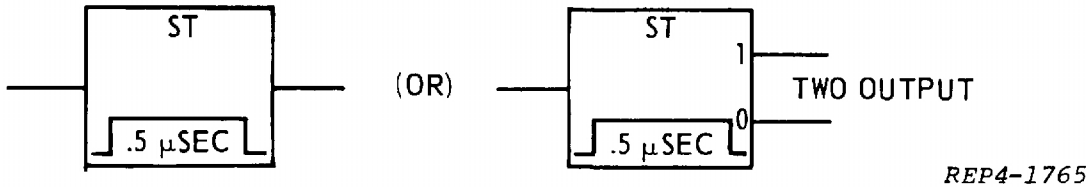

Figure 6-11. Schmitt Trigger Symbols

The Schmitt trigger (ST) function symbols are shown in figure 6-11. The ST is actuated when the input signal crosses a certain *threshold* voltage. Output signal amplitude and polarity are determined by the circuit characteristics of the ST and not by the input signal. Waveforms may be shown inside or outside the symbol, indicating amplitude, polarity, threshold voltage, and duration. The unactuated state of ST is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state as long as the input exceeds the threshold value.

Compare the symbols of the FF, SS, and ST. Notice how inputs and outputs are indicated. The FF symbol is rectangualr in shape, and the SS and ST symbols are square.

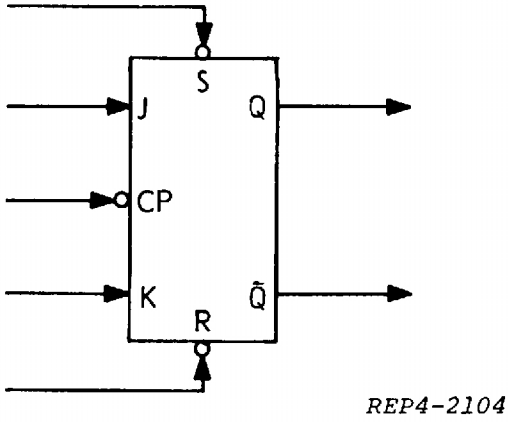

Figure 6-12. Logic Symbol for JK Flip Flop

JK FLIP FLOP

The development of the JK flip flop has made possible a wide variety of applications because of the flexibility of their control modes. There are several basic circuits that can be assembled using one or two JK flip flops and there are an unlimited number of ways several JKs can be connected. Some of the more common circuits that use JK flip flops are binaryy counters, shift registers, and ring counters.

The JK flip flop is a basic bistable multivibrator with certain modifications which make it extremely adaptable for digital circuits. It is the most extensively used of all the flip flops because of its adaptability. It may be employed as an up or down counter, ring counter, and storage or shift register. Figure 6-12 shows the logic symbols for the JK flip flop with direct set and reset inputs.

J	K	CP	FF
L	L	DOWN CLOCKS	NO CHANGE
L	H		RESET Q LOW $\bar{Q}$ HIGH
H	L		SET Q HIGH $\bar{Q}$ LOW
H	H		COMPLEMENT

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Figure 6-13. Truth Table for JK Flip Flop

The condition (set or reset) of the JK flip flop is controlled by the inputs J, K, CP, S, and R. INputs S and R are the direct set and reset inputs, respectively. Anytime one of these input levels goes low (down clock), the J and K inputs will be inhibited. If the set input (S) goes low, the set side output of the flip flop (Q) will go high. When Q is high, $\bar{Q}$ will be low. If the reset input (R) goes low, the reset side output ($\bar{Q}$) will go high. When $\bar{Q}$ is high, Q will be low. In other words, inputs S and R make it possible to directly set or reset the flip flop regardless of the input levels present at J, K, and CP.

When both direct set and reset inputs are high, the condition of the flip flop is determined by the gated input levels J and K and the clock pulse (CP). Refer to the truth table (figure 6-13) for the four possible input levels at J and K.

INPUTS				OUTPUTS	
PRESET	CLEAR/RESET	D	CP	Q	$\overline{Q}$
L	H	L/H	L/H	H	L
H	L	L/H	L/H	L	H
H	H	H	U/C	H	L
H	H	L	U/C	L	H

Figure 6-14. Truth Table for D Flip Flop

The four possible conditions as shown in the truth table are:

1. When J and K are both low and there is a down clock at the CP input, the condition of the flip flop will not change. That is, if the flip flop were previously set, it will remain set; if it were previously reset it will remain reset.

2. When J is low and K is high and there is a down clock at the CP input, the flip flop will reset: Q will be low and Q will be high.

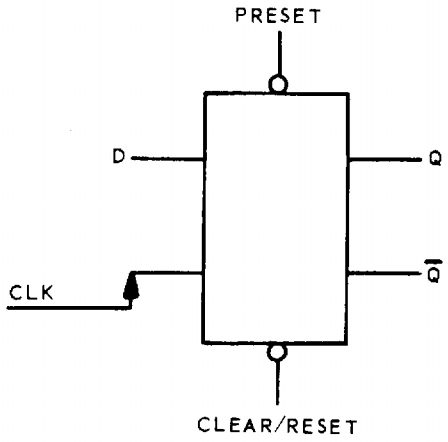
3. When J is high and K is low and there is a down clock at the CP input, the flip flop will set: Q will be high and Q will be low.

4. When J and K are both high and there is a down clock at the CP input, the flip flop will complement. That is, it will assume the opposite state it was previously in.

D FLIP FLOP

These monolithic low power, dual edge triggered flip flops utilize TTL circuitry to perform D type flip flop logic. (Refer to figures 6-14 and 6-15.) Each flip flop has individual clear and preset inputs, and complementary Q and Q outputs.

A positive going transition at the CP input transfers the level at the D input to the Q output with the complement of this level appearing at the Q output.



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Preset: A low on the preset causes Q to go high.

Reset/Clear: A low on the preset causes $\overline{Q}$ to go high.

NOTE: Preset and clear override anything that may happen on the D or clock input.

Figure 6-15. D Type Flip Flop

DECIMAL - NUMBER OF INPUT PULSES	BINARY - STATE OF FLIP-FLOP DCBA
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111 = MAXIMUM COUNT
16	0000 = CLEAR
17	0001 = COUNT STARTS OVER

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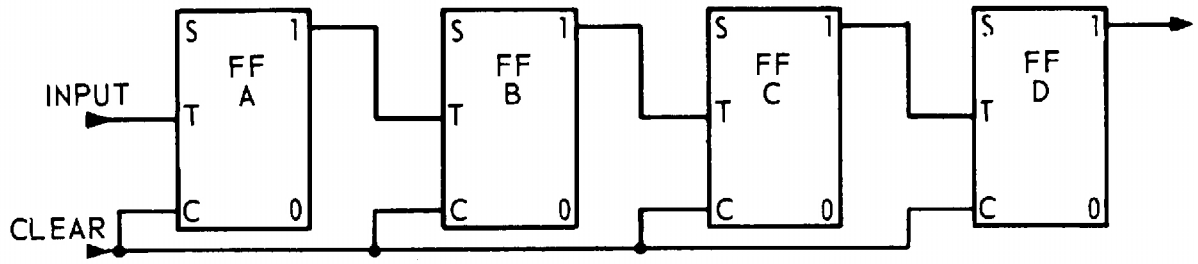
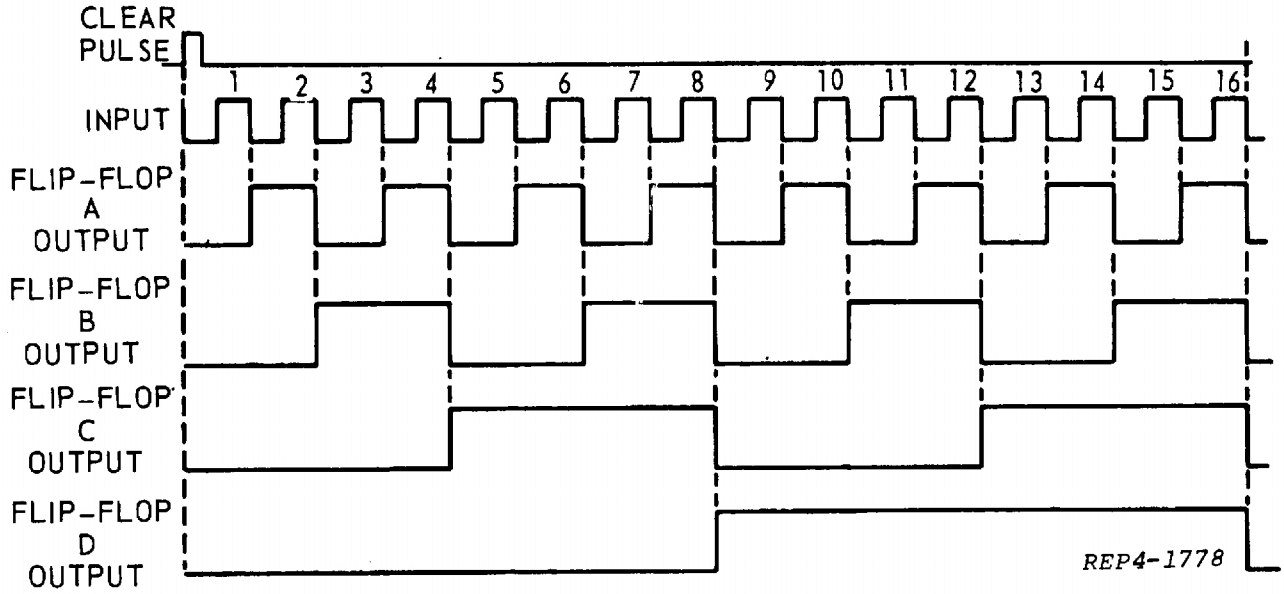
Figure 7-1. Count Table



A. SYMBOL



B. WAVEFORM CHART

Figure 7-2. Serial Up Counter (Down Clock)