Chapter 8

SPECIAL CIRCUITS

ONE-OF-EIGHT DECODER

The 1/8 decoder, figure 8-1, provides a logic one on the single decimal output of the device corresponding to the 3-digit binary number that is applied to its input. All other outputs will be logic zeros. Input A0 is the least significant digit.

PARALLEL-TO-SERIAL CONVERTER

The parallel-to-serial converter, figure 8-2, is a device that has eight parallel inputs (I0-I7). One of these inputs is selected as the output of the device by the weighted binary selection lines S0-S2. The decimal numbered input that corresponds to the binary number at the selection lines is "switched" to the output. For example, when S0, S1 and S2 are respectively 110 (S0 is the least significant digit, I3 is switched to the output. The device is enabled with a logic zero or inhibited with a logic one applied to the E input.

FAN IN GATE

The "fan in gate," figure 8-3, is a device that can be made to select one of four data sources as an output. Each of these data sources is applied to one input of a dual input AND gate. The remaining input to each AND gate is the enable/inhibit control for the associated gate and requires a logic one to enable it. Data is selected by applying logic zeros (inhibit) to three of the control lines and a logic one to the control line of the desired AND gate.

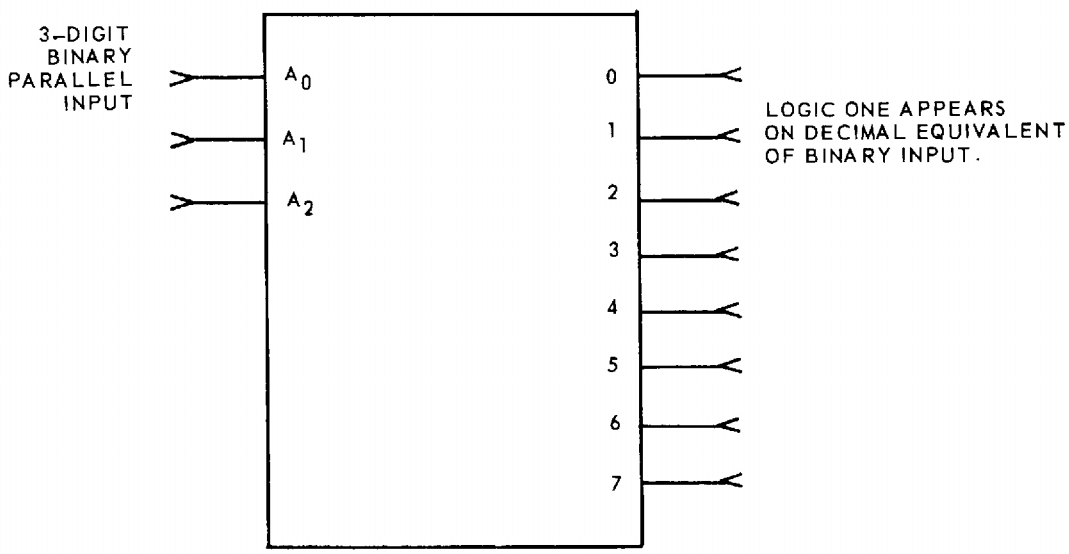


Figure 8-1. One-of-Eight Decoder

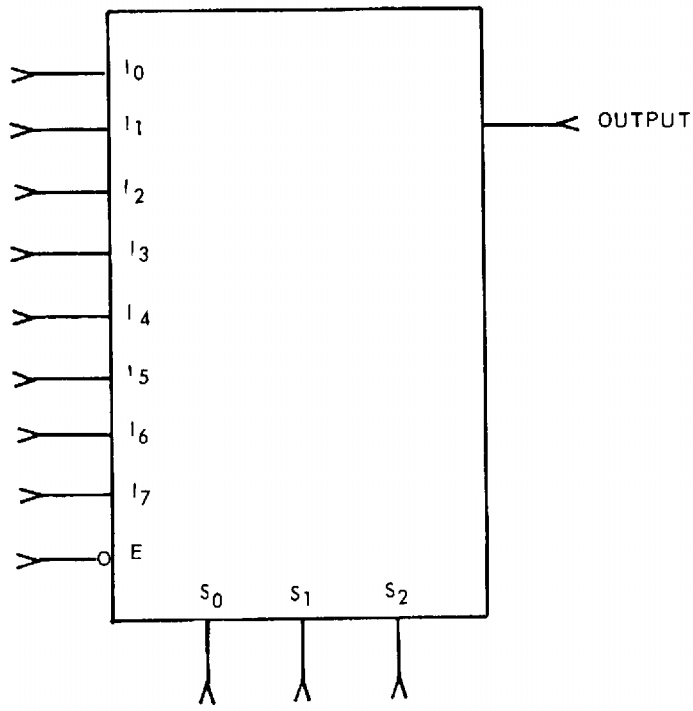


Figure 8-2. Parallel-to-Serial Converter

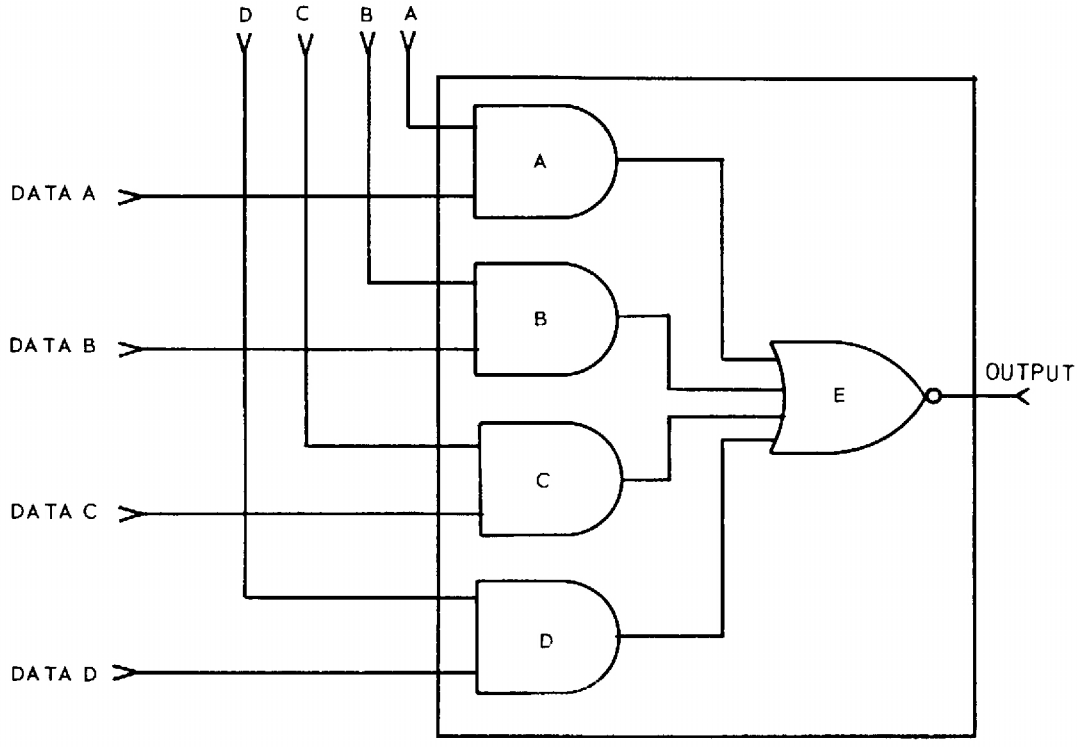
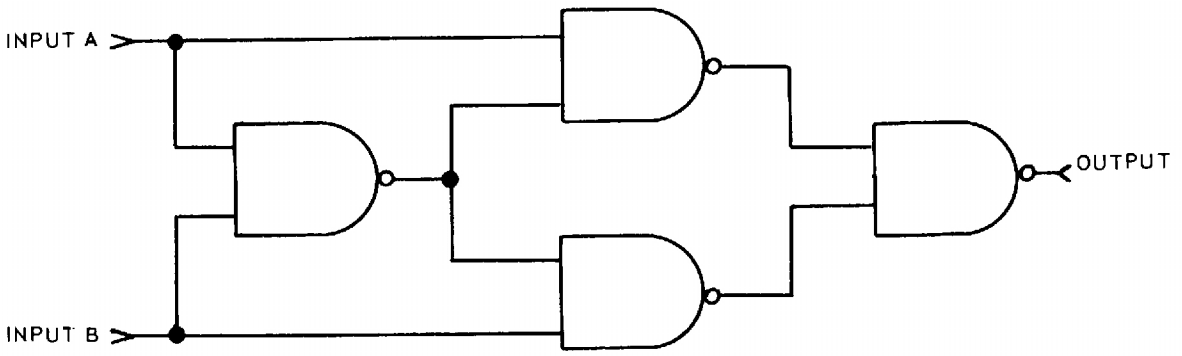


Figure 8-3. Fan In Gate



1. VERIFY: IF A = B, OUTPUT = "0"
2. INVERTER: IF B = "1" AND A = DATA, OUTPUT = $\overline{\text{DATA}}$
3. NONINVERTER: IF B = "0" AND A = DATA, OUTPUT = DATA

Figure 8-4. Verifier/Inverter

VERIFIER/INVERTER

The verifier/inverter circuit, (figure 8-4), when used as a verifier, has two data sources applied to its inputs. The output will be a logic zero, provided the logic levels at the inputs agree. When the inputs are not in agreement, the output is a logic one.

The same circuit configuration can be used to determine whether *one* source of data is *output* in its true form or in the inverted state. This is accomplished by applying data to one input and selectively applying a logic one or a logic zero to the remaining input. A logic one causes the data to be output in its inverted form.

NOTES