MODULE 25
887B-1 ELECTRICAL FREQUENCY SYNTHESIZER OPERATION

OBJECTIVE

Explain the operation of the 887B-1 Electrical Frequency Synthesizer.

PREREQUISITES

Must complete Modules 1, 2, 3, 15, 20, and 21.

INFORMATION

The 887B-1 Electrical Frequency Synthesizer, commonly called the synthesizer or the 887B-1, performs two important functions in the Receiver and the Transmitter. It provides the DCU and DCFE circuits that interface the Receiver or Transmitter with the controlling computer, and it provides all the required injection frequencies to operate the Receiver or Transmitter. The TO for the 887B-1 is 31R2-2GR-1052. Read para 4-1 thru 4-10 of that TO before continuing.

Remember, there is more than one DCU circuit on the computer control bus. In order for the computer to distinguish to which DCU a particular control word is being sent, bits 1 through 5 of the word contain an address. The address strapping for the 887B-1 is **not** in the black box. This is because the box could be placed in any one of four positions: Receiver 1, Exciter 1, Receiver 2, or Exciter 2. So, the address strapping is done on the shelf that the 887B-1 is plugged into. Consequently, any 887B-1 plugged

into any of the four positions will contain the proper addressing.

Look at the block diagram in Figure 17 of your Diagrams booklet. On the left side of the diagram you see the five address lines coming into the DCU along with the control bus and carrier bus (clock). The monitor bus comes from the same DCU on its way back to the computer. The block diagram shows the control bus and carrier bus going to the DCU modulator card, A6. The signal is not processed in this card. It simply passes through to the demodulator circuit, A7. The demodulator converts the bi-phase modulated sine wave back to logic level data. This is accomplished for both the clock and the control data. The logic level clock output is called DCFE bit clock and is used for timing throughout the DCU/DCFE .

The control data is sent back to the modulator card, where the address bits are compared with the address strap lines. If the address compares, the control gate line is enabled, and the remaining bits of the control word are processed by the DCFE. The outputs of the DCFE going to the rest of the Receiver are shown on the left edge of the diagram. Let's discuss those outputs.

First is the information from control word I. Control word I is frequency information that is sent to the 888B-2 for its tuning. Notice that only six lines are sent out. That's because the 888B-2 coarse-tunes in 1MHz steps. Fine tuning depends on the injection frequency which comes from the synthesizer portion of the 887B-1. We'll discuss how this occurs later.

Looking at Figure 17 again, you see that some of the control bits from the DCFE are shown individually, and some are grouped together like the frequency lines we just

observed. For an individual accounting of each of the lines, refer to Figure 4-7 in the TO. Using this drawing you can trace the absence of any individual control signal to the gate it is supposed to come from.

For example, let's say your Receiver won't accept changes in squelch settings. Looking at Figure 4-7, you can see that the squelch word for the A sidebands goes through A3U5, and for B sidebands the data goes through A3U2. As we've discussed before, if you or your unit have the capability to repair the defective circuit card (equipment and skills), then by all means troubleshoot to the defective component and repair it. If you do not have the capability, you are authorized to simply replace the defective card. In the latter case, there's obviously no need to troubleshoot below the defective card. Now let's take a look at the synthesizer.

Like most synthesizers in use today, the synthesizer used in the TSC-60 is made up of phase-locked loops (PLLs). In a PLL, the desired frequency is locked to a very stable, accurate frequency standard. If the circuit only requires a single frequency, the simplest solution is to make the standard that desired frequency, and that is the end of it. However, if the output needs to be a variable frequency, or you need more than one output, having a standard for each frequency becomes cost prohibitive. This is where a PLL earns its keep. Take a look at Figure 25-1.

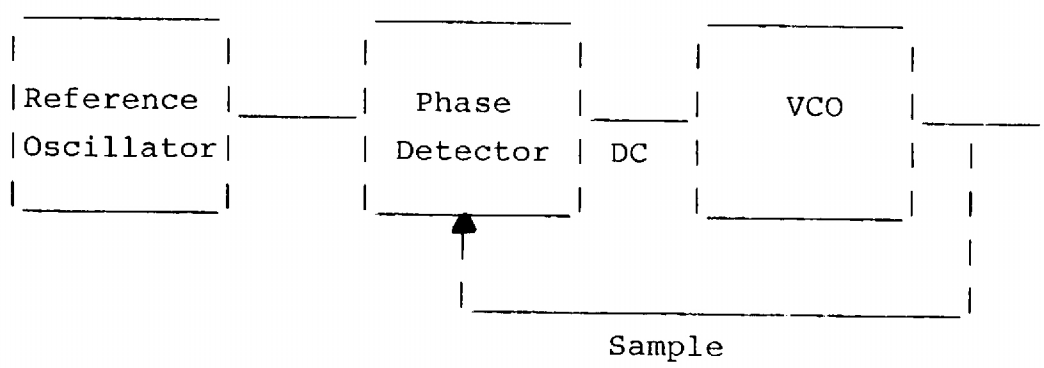

Figure 25-1. Simple Phase-Locked Loop

The output of the frequency standard, or reference oscillator, is fed to a phase detector. The output of another oscillator, the VCO (Voltage Controlled Oscillator), is sampled and sent to the other input of the phase detector. The phase detector compares the two signals and produces a DC voltage that varies according to the difference in the two input signals. This DC voltage is applied to the VCO. In a VCO, the output frequency varies with a DC input voltage. The DC voltage coming from the phase detector drives the VCO to change its frequency to equal the reference oscillator frequency.

If the output frequency of the VCO drifts, the phase detector will see the difference between the sample and the output of the reference oscillator and change the DC input to the VCO again to correct it. The end result is that the output of the VCO is just as accurate and stable as the reference oscillator.

We said previously that the PLL doesn't pay for itself unless the frequency needs to be variable or more than one frequency is needed. Let's now see how both of those results are obtained. Look at Figure 25-2. This diagram indicates that we have two frequencies, 8MHz and 16MHz, that are both phase-locked to one reference oscillator. By

dividing the sample frequencies, they can be compared with the reference frequency. This provides stability and accuracy of the reference oscillator for two different output frequencies. If the frequency divider were variable, the output frequency would be variable while still maintaining the stability of a fixed reference. These two basic techniques, along with standard mixing and multiplying, are employed in the 887B-1 synthesizer to obtain the desired output frequencies.

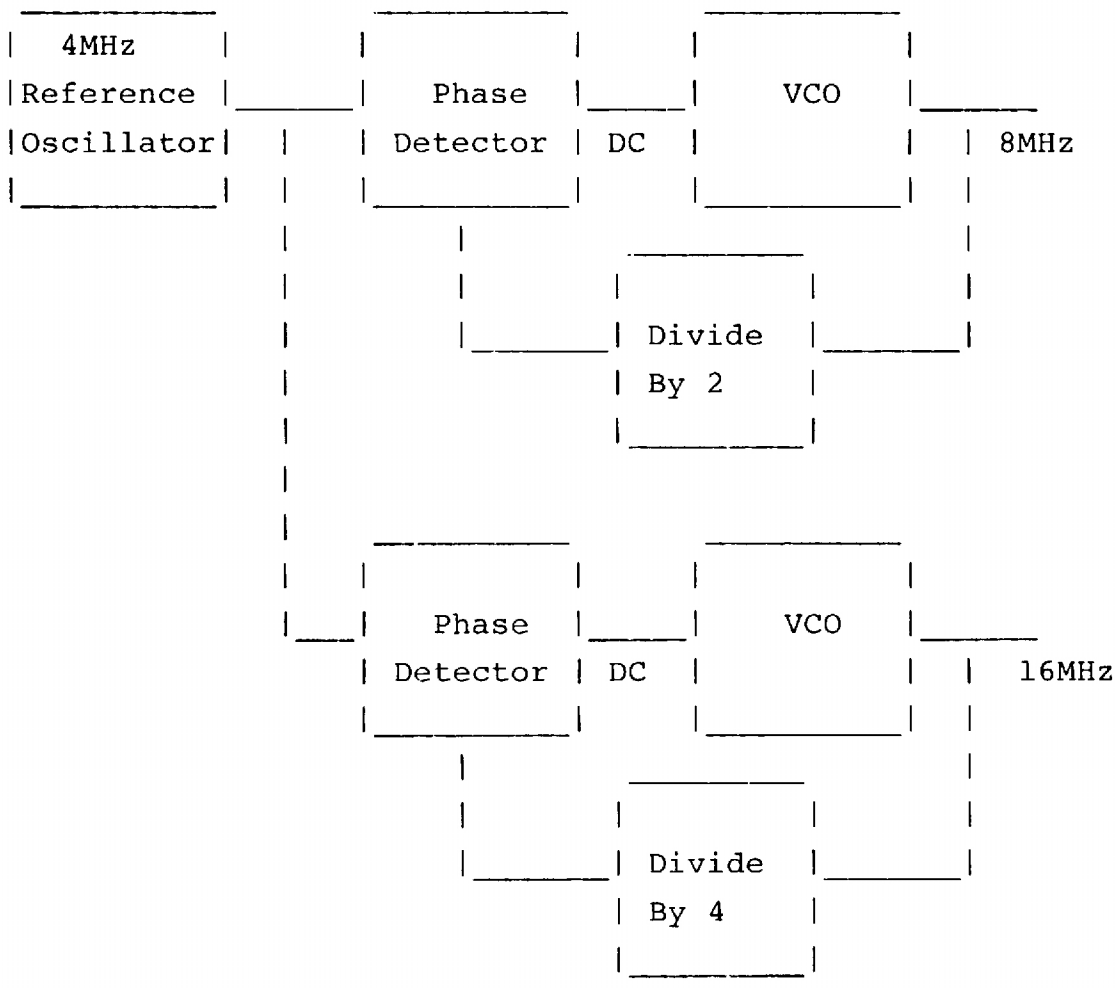

Figure 25-2. Typical PLL Circuit

Look at Figure 17 in the Diagrams booklet. This synthesizer contains six PLLs referenced to an internal 4MHz reference oscillator: 9.9MHz, 243.710kHz, 250.000kHz, 256.290kHz, 10kHz, and 9.9kHz. Two of these loops (9.9kHz and 10kHz) are used to generate the variable injection (79.1501 to 107.1500MHz) frequencies in 100Hz steps.

The 4MHz frequency standard module produces 100kHz. This 100kHz is fed through an electronic switch to the phase detector for the 9.9MHz PLL. The switch allows you to use an external 100kHz standard. Remember the eight BNC connectors on the top of the Receiver/Exciter Rack? Four of those couple the 100kHz standard to the input of the four 887B-1s. The other four couple the 100kHz outputs from the four 887B-1s, but those do not come directly from the reference oscillators. Instead, they come from a divide by 99 circuit in the 9.9MHz PLL. The external 100kHz connectors allow you to remain in operation even though a 4MHz oscillator module has failed. If the electronic switch senses 100kHz from the external 100kHz connector, it automatically switches the external signal to the phase detector.

The 100kHz from the 4MHz reference oscillator module is fed to the 9.9MHz PLL. The 9.9MHz PLL produces 9.9MHz and 100kHz. These two frequencies are used by the rest of the PLLs as references. First, the 100kHz goes to the 250kHz PLL. This produces the 250kHz signal used in the RF translator for tuning. The 250kHz is also applied to the 6.29kHz PLL. This circuit is actually two PLLs on one circuit card. Let's discuss the 256.29kHz PLL first.

The 250kHz is mixed with the 256.29kHz to produce a difference frequency of 6.29kHz. The 9.9MHz from the 9.9MHz PLL is divided by 1574 to produce 6.29kHz, which is used as a reference. The two 6.29kHz signals are compared in the

phase detector, and the result is the DC tracking signal for the 256.29kHz VCO. The other PLL on this circuit card is similar to the 256.29kHz PLL, except the 250kHz is mixed with 243.71kHz to produce the 6.29kHz difference. The 256.29kHz and 243.71kHz signals are used by the 889A-2 IF translator to demodulate the A2 and B2 sidebands.

The 9.9MHz reference is multiplied by 10 in the X10 multiplier circuit to produce the 99MHz injection frequency. That takes care of all the fixed injection frequencies produced by the 887B-1. Now, let's discuss the variable injection.

You should recall from our discussion of the RF translator that the variable HF injection frequency is controlled so that when it is mixed with the operating frequency, the sum will equal 109.15MHz. So, if the operating frequency is 2.00000MHz, the injection frequency will be 107.15MHz (109.15-2.00=107.15). If the operating frequency is 29.99999MHz, the injection frequency will be 79.15001MHz (109.15-29.99999=79.15001). You need to remember this formula in order to determine whether the variable HF injection frequency is correct or not.

The variable HF injection frequency is derived from the 10kHz PLL and the 9.9kHz PLL. Determining what frequency these two loops should be operating at is not nearly as easy as determining the frequency of the variable injection signal. To determine these two frequencies, use the following steps:

1. Determine the variable HF injection frequency.
2. Compute the 10kHz PLL divider (division ratio).
3. Multiply the result of Step 2 by 10kHz and subtract the result from 99MHz. This difference will be the 10kHz PLL output frequency.

4. Subtract the 10kHz PLL output frequency from the variable injection frequency. The difference is the 9.9kHz PLL output frequency.
5. Compute the 9.9kHz divider (division ratio).
6. Divide the result of Step 5 by that of step 6. The result should be 9.9kHz.

Let's next consider an example by assuming an operating frequency of 7.8615MHz.

First, you need to determine the variable HF injection frequency:

109.15MHz - 7.8615MHz = 101.2885MHz

Second, you compute the 10kHz PLL division ratio as shown below:

	MHz		100 kHz	10 kHz	1 kHz	100 Hz
Operating Frequency	7	.	8	6	1	5
Move 1kHz and 100Hz digits			1	5		
Add fixed number	3		7	1		
Total	10		16	12		

Determine the division ratio by adding the totals as follow:

```
          10  =  1000 (add two zeros to the first number)
          16  =   160 (add one zero to the second number)
          12  =    12
         ------------
Division ratio  =  1172
```

Third, you multiply the division ratio by 10kHz and then subtract the result from 99MHz to obtain the output frequency of the 10kHz PLL:

1172 X 10kHz = 11.72MHz
99 MHz - 11.72MHz = 87.28MHz = 10kHz PLL output

Fourth, to obtain the 9.9kHz PLL output frequency, you subtract the 10kHz PLL output from the variable HF injection frequency:

101.2885MHz - 87.28MHz = 14.0085MHz

Fifth, you compute the division ratio for the 9.9kHz PLL. This is done by adding the number 1400 to the last two digits (1kHz and 100Hz) of the operating frequency:

Operating frequency = 7.8615MHz
1400 + 15 = 1415

Sixth, you divide the operating frequency of the 9.9kHz PLL by the division ratio you just came up with, and the result should be 9.9kHz:

14.0085MHz divided by 1415 = 9.9kHz

It works. But why go through all that "goat roping?" The answer is simple: If a PLL is not putting out the

correct frequency, you must know how it is supposed to obtain that frequency in order to troubleshoot it.

ADDITIONAL INSTRUCTIONS

Answer the review questions and check your answers with the confirmation key. Review the module for any questions you missed. Next, ask your trainer for the KEP questions. After your trainer checks your answers and reviews the questions missed with you, he/she will assign you another module.

REVIEW QUESTIONS

1. For an operating frequency of 15.245MHz, what is the required variable HF injection frequency?

2. Where is the DCU address strapping located, and why is it there?

3. All the outputs of the 887B-1 are stable, but slightly off frequency. What is the most likely problem?

4. Describe the function of a VCO and a phase detector in a basic phase-lock loop circuit.

You may refer to the STM Module for the following question.

5. Compute the output frequencies of the 10kHz and 9.9MHz phase lock loops with an operating frequency of 8.225MHz.