Chapter 12

ROM COMPUTER

INTRODUCTION

Control-Monitor Group OK-145/TSC-60(V) consists of Transmitter Control C-8363/TSC-60(V) (transmit control head), Receiver Control C-8362/TSC-60(V) (receive control head), and Control-Monitor C-8364/TSC-60(V) (audio control unit). The three-unit combination controls and monitors a selected radio equipment group. The transmit control head contains a computer. This section is about the computer, which consists of only five circuit cards and yet is the nucleus of the entire radio group.

Hardwire Memory Card A7A2

The Hardwire Memory Card stores the computer program. Specific program steps or *instructions* are selected by the Instruction Address Counter (IAC). In addition, this card contains the ACCUMULATOR (Location 0) and the instruction verify circuit.

Instruction Decode Card A7A5

The Instruction Decode Card interprets all program instructions and controls the routing of data accordingly. The arithmetic and logical operation circuits are also part of this card.

Accessible Memory Card A7A6

The Accessible Memory Card, oddly enough, contains *accessible* storage locations. That is, the program determines when data is put into these registers, what data is input, and how this data is used. The register array, or *data bank*, consists of 16 registers, each capable of storing 32 bits.

Processor Card A7A4

The Processor Card generates the *time base* for all computer operations except the interval of time when data is being exchanged with a DCU. The data rate established and controlled by this card is 250/kilo-bits/sec.

CCCS Timing Card A7A3

The CCCS Timing Card establishes the 4800 bits/sec data rate required when data is exchanged between the computer and a DCU. It also provides the input to the fault register, Location 16 on the Accessible Memory Card.

Computer Operation

This section deals entirely with how the five cards of the computer interact to perform individual program instructions.

INSTRUCTIONS

Each step of the computer program is executed as a result of a "Command" from the Hardwire Memory Card A7A2. These commands are permanently stored in a matrix and are read out and accomplished one at a time in a predetermined sequence. The types of commands and their sequence was established by the person who wrote the program. In other words, these commands and their sequence *are* the computer's program.

In the AN/TSC-60(V) computer, these commands are in the form of a 16-bit instruction words. Since the computer, like a person, must first *read* an instruction, then *remember* it while doing the task, these instruction words are loaded into an "Instruction Memory Circuit" *prior* to execution and then discarded immediately following the execution interval.

The time required to read, execute and discard one instruction is called a "Computation Cycle". This cycle is further divided into "Frames" which correspond to the activity being accomplished. The "Read" frame is 32 counts (bits) long. The "Process" frame (Instruction Execution) is 32 counts long and the "Increment/Load" or "Reset" frame (discard) is 8 counts long. Thus, the *basic* computation cycle is a total of 72 counts. To accomplish one program step the computer must "Read" the instruction during counts 0-31, "Process" that instruction during counts 32-63, and finally "Reset" itself for the next computation cycle during counts 64 - 71. (Count 71 is immediately followed by count 0 of the next cycle.)

To accomplish the entire program, the computer simply repeats the cycle of read, process and reset until all program steps have been accomplished. Note that there is virtually no "end" to the program because the last program instruction causes the computer to *repeat* the entire program.

Instruction Sets (OP-Codes)

The sixteen computer functions or operating modes are individually selected by bits 13 through 16 of the instruction word. These four bits are referred to as the "OP-CODE". The following discussion explains these sixteen op-codes and is keyed to Table 12-1.

0: LDRD, LOAD DATA REGISTER DIRECT. The computer makes a request on the Logic Level Control Bus to either the Transmit or Receive Control Head for one of six Logic Level Monitor Words and inputs the requested word (Frequency, Mode, or Squelch/Carrier Level) via the Logic Level Monitor Bus to a selected Accessible Memory Location (Data Register).

1: OUTD, OUTPUT DIRECT. The computer outputs a *Control* Word from a selected data register via the Logic Level Control Bus to the front panel lamps of either the Transmit or Receive Control Head.

2: OUTS, OUTPUT SINEWAVE. A selected data register is output on the CCCS Bus to a specific DCU (Device Control Unit) and the returning Monitor Word from the DCU is stored in a separate selected location.

3: EORD/LORD/STRD/STR-R. All of these operations have the same OP-CODE, however, certain other bits of the Instruction Word act as *Modifiers* to determine the specific operation to be performed. The function this OP-CODE performs is to cause the Accumulator's (Location "0") input and output data to be available for a variety of applications as determined by the previously mentioned modifier bits. These selected operations are as follows:

a. EORD, Exclusive or Direct. The logical operation of EOR is performed between a selected data register and the Accumulator's content.

b. LORD, Logical or Direct. The logical OR operation is performed between a selected data register and the content of the Accumulator.

c. STRD, Store Direct. The content of the Accumulator is input to a selected data register.

d. STR-R, Store Register. The content of a selected data register is input to the Accumulator.

4: STR-F, STORE FAULT. Enables the content of the Fault Register (Location 16) to be input to a selected data register.

5: COZ, CONDITIONAL ON ZERO. A specific bit of a selected data register is checked for the presence of a zero and if so, a Branch Load Frame is generated.

6: CNZ, CONDITIONAL, NON-ZERO. A specific bit of a selected data register is checked for the presence of a one (non-zero) and if so, a Branch Load Frame is generated.

7: BNZ, BRANCH, NON-ZERO. The entire content of a selected data register is checked for the presence of a one (non-zero). If any bit is a one, a Branch Load Frame is generated.

8: BPZ, BRANCH, PROGRAM ZERO. The Accumulator is loaded with a Branch Address from a selected data register during the *Process* Frame. This is an *Unconditional* Branch.

9:LDRL, LOAD DATA REGISTER, LITERAL. A selected data register is loaded with a binary *Literal* from the Hardwire Memory Card.

10: SELF CNT/SELF RESET. The Radio Group Counter is either advanced in count by one or is master reset, depending on the state of a specific modifier bit.

11: EORL/LORL/ANDL. The logical operation of "OR", "EOR" or "AND" is performed between a selected data register and a binary Literal. The specific operation performed is selected by modifier bits.

12.MOZ, MODIFY TO ZERO. A specific bit of a selected data register is forced to the zero state.

13: MNZ, MODIFY TO NON-ZERO. A specific bit of a selected data register is forced to the one state.

14: ROT, ROTATE. The content of a selected data register is shifted a specified number of bit positions to the right. No data is "lost".

15: ADD. The content of a selected data register is summed with a binary Literal (used only in the Diagnostic Program).

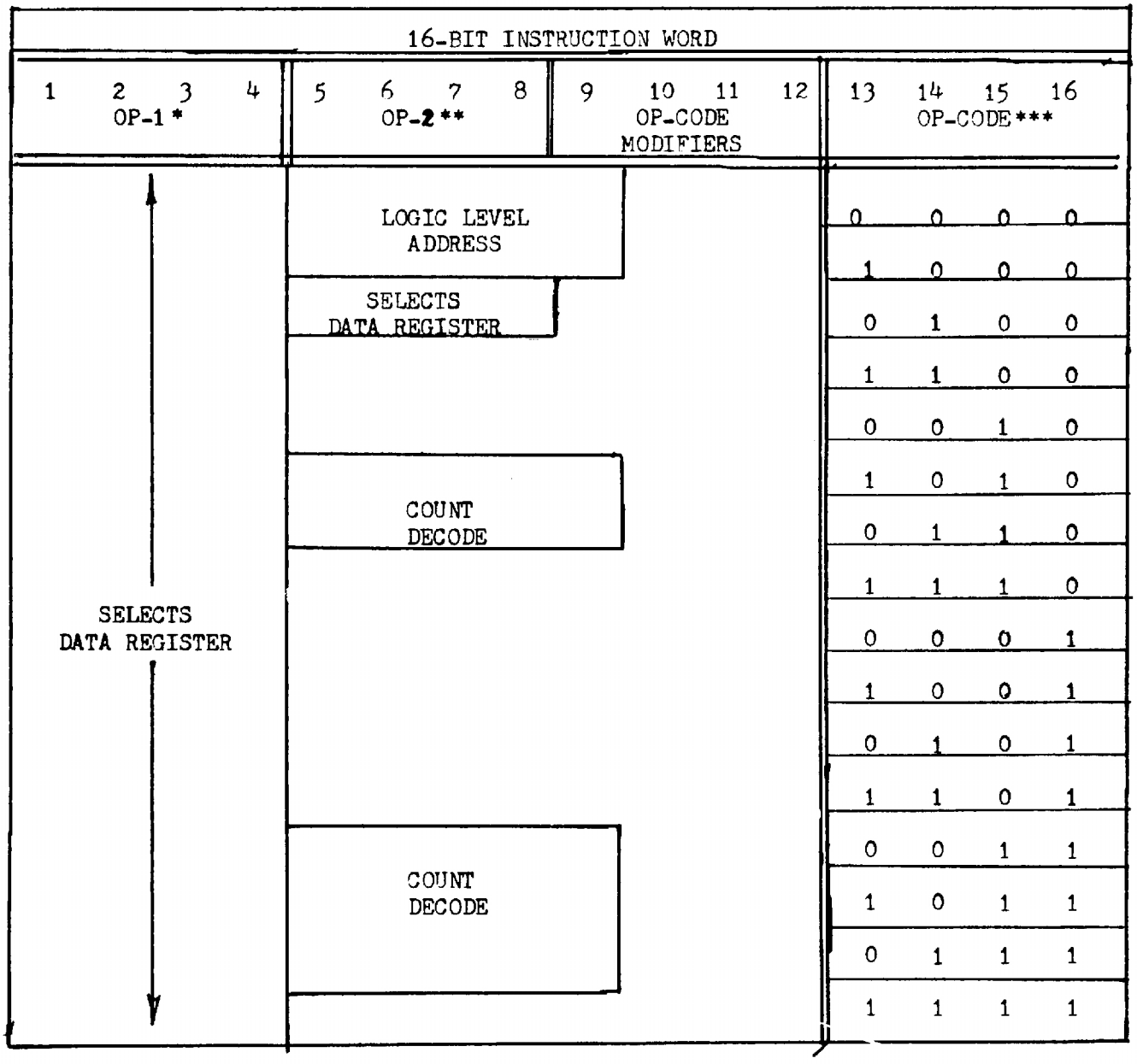
A more detailed explanation of the computer's operation requires an understanding of how the Instruction Word performs its control functions.

Table 12-1

INSTRUCTION SETS			
OP-CODE	DEC EQV	OPERATION	* REQUIRED MODIFIERS
0000	0	LDRD	NONE
1000	1	OUTD	12 = 1
0100	2	OUTS	10 = 1
1100	3	EORD; LORD; STRD; STR-R	9,10&12=1; 8,10&12=1; 10=1; 10,11&12=1
0010	4	STRF	NONE
1010	5	COZ	12=1
0110	6	CNZ	12=1
1110	7	BNZ : LOC 1—15; LOC C	12=1 ; 10,11&12=1
0001	8	BPZ	10,11&12=1
1001	9	LDRL	5=0/1, 6=0/1
0101	10	SELF CNT; SELF RESET	8=1; 7=1
1101	11	EORL; LORL; ANDL	9,10&12=1; 8,10&12=1; 7,10&12=1, 6=0/1
0011	12	MOZ	NONE
1 11	13	MNZ	NONE
0111	14	ROT	12=1
1111	15	ADD	12=1, 6=0/1

Bit 5 - Determines whether 1's or 0's are loaded into the non-selected half of a data register. If Bit 5 is a 1, 1's will be loaded.
Bit 6 - Selects the right or left half of the data register. If Bit 6 = 1, right half.
Bit 7 - Enables self reset or selects "ANDL".
Bit 8 - Enables slef count or selects "LORL" or selects "LORD".
Bit 9 - Selects "EORL" or selects "EORD".
Bit 10 - Causes the Accumulator to be clocked during the Process Frame.
Bit 11 - Causes the Accumulator to *also* receive the Data Bank Input (DBI).
Bit 12 - Enables the Data Band Output (DBO) to be recirculated to the DBI.

Table 12-2



* The function of OP-1 remains the same for all OP-CODES; it selects one of fifteen storage locations on the Accessible Memory Card or the Accumulator.

** The function of OP-2 varies and is dependent upon the OP-CODE.

*** Refer to the text and Table 12-1 for an explanation of the function of each OP-CODE.

INSTRUCTION MEMORY CIRCUIT

The Instruction Memory Circuit consists of four 4-bit storage registers A6, A7, A8 and A12 located on the Instruction Decode Card A7A2 (KCS-5272). The 16-bit Instruction Word is serially input tothese registers during the Read Frame and appears during the Process Frame as static parallel "1's" and "0's" which are used in the following manner.

OP-CODE, Instruction Bits 13 - 16

The four bits stored in Register A12 determine the "Operating Mode" of the computer and are known as the *OP-CODE.* The OP-CODE determines the *type* of operation to be executed during any given computation cycle. These four bits are applied to 1 of 16 Decoder A13 (adjacent to A12) causing one of the sixteen different computer operations to be selected (0000-1111). Refer to Table 12-1 for the specific operation enabled by each of the sixteen possible codes.

The remaining twelve bits of the Instruction Word provide the necessary additional information required by the computer to perform the selected operation.

OP-1, Instruction Bits 1-4

The four bits stored in Register A7 are known as Op-1 and are extended to the Accessible Memory Card A7A6 (KCS-5272). They are interpreted as weighted inputs to a Count Decoder and select the specific 32-bit register that will be clocked during the Process Frame.

OP-2, Instruction Bits 5-8

The four bits stored in Register A6 are known as Op-2 and can perform several unrelated functions depending on which *operation* is selected by the *OP-CODE.* In order to accomplish these different functions, the four bits are extended in parallel to several different devices, only one of which will be enabled for a specific operation. These devices and the associated functions are as follows:

1. When the operation is LDRD or OUTD (OP-CODE 0 or 1), OP-2 is applied to Multiplexer A11 and determines 4 bits of the 5-bit Logic Level Address.

2. When the operation is OUTS (OP-CODE 2), OP-2 is extended to 4-bit register A5 on the Accessible Memory Card A7A6 and selects the storage location for the first returning CCCS Monitor Word.

3. When the operation is a conditional branch, modify bit, or ROTATE (OP-CODES 5,6,12,13 or 14), OP-2 provides 4 of the 5 weighted inputs to Count Decoder A15. The function of A15 is to signal a specific count/bit interval within the Process Frame.

4. During certain other operations, selected OP-2 bits act as modifiers to the OP-CODE. See Tables 12-1 and 12-2.

OP-CODE MODIFIER, INST. BITS 9-12

The four bits stored in register A8 are collectively referred to as the OP-CODE MODIFIER. These bits are used independently as modifiers to the OP-CODE.

Bit 9 (A8 pin 6) performs several unrelated functions depending on the operation selected by the OP-CODE.

1. It is applied to the A11 Multiplexer and determines one bit of the 5-bit Logic Level Address.

2. It is applied with WT 16 to Count Decoder A15.

3. It is applied to NAND Gate A1B as a "1" to select the EOR function if the operation is OP-CODE 3 or 11.

Bit 10 (A8 pin 8) is extended to the Processor Card A7A6 and enables or inhibits the Accumulator Clock during the Process Frame.

Bit 11 (A8 pin 11) is applied to the Accumulator input Fan Gate A18 as a logic one to gate DBI data to the Accumulator.

Bit 12 (A8 pin 13) is applied to DBI Fan Gate A23 as a logic one to enable recirculated DBO to become DBI. Bit 12 is also inverted and applied to NAND Gate A4B. The result is that when the selected operation is OP-CODE 3 and Bit 12 is a logic zero, DBI Fan Gate A22 will gate S1 data (the serial output of the Accumulator) to the DBI.

INSTRUCTION EXECUTION

Referring to the block diagram of the ROM computer in the student diagram book, let's see how

the computer reads out an instruction word from the hard-wired memory, executes the instruction, and then goes to the next step in the computer program.

The first thing that occurs during the instruction execution cycle is to read the instruction addressed by the Instruction Address Counter (IAC), into the Instruction Register. Program readout is verified by reading each instruction from the hard-wired memory twice.

The first 16 clock pulses of a group of 32 load the Instruction Register. The second 16 clock pulses causes the contents of the Instruction Register to be serially shifted back around and compared to the second readout of the same fixed wired memory location. If the comparison is negative, the processor timing element automatically resets the IAC.

Once the instruction is in the Instruction Register, it can be executed. The OP Code bits will then be decoded to determine the type of operation to be performed. The OP Code modifier bits will be used primarily to enable certain functions and to select the designated data paths that are necessary to execute the particular instruction. The OP 1 and OP 2 fields will be used primarily to select location of the accessible memory.

ACCESSIBLE MEMORY

The accessible memory is a serial-in/serial-out register array consisting of 16 storage locations, each containing 32 bits. This memory provides storage for control data, which is to be output, or monitor data, which has been input and is to be analyzed. The data contained in these locations is under program control; i.e., OP 1 and OP 2 designate these locations.

PROCESSOR TIMING

The processor card provides the internal timing for the computer. A time cycle, the largest repetitive interval, consists of either three or four frames. These frames are defined below.

Instruction Read Frame (Group A)

The instruction read frame is the first frame in the cycle and is 32 bits wide. During this interval, instruction data (MDO on the hard-wired memory card) is shifted to the instruction storage register (Instruction Decode Card) with the timing provided by the Instruction Storage Clock (INC). The 16 bits of instruction data are scanned twice during the 32-bit interval. One negative pulse occurs on Instruction Address Counter Clock (IAC CLK) during the 30th bit clock of INC. This is necessary in order to increment the IAC to the next program step.

Process Frame (Group B)

The process frame is the second frame in the cycle and is 32 bits wide. During this frame, the instruction that was read in the instruction frame is carried out. Data from either the accessible memories or the accumulator is shifted from the Data Bank Output (DBO) from the accessible memory card, through the instruction decode card. Accessible memory data, if selected, is shifted with Data Bank Clock (DBC). The DBC signal ALWAYS and ONLY appears during the process frame, even though accumulator data is selected for DBO. If the accumulator is selected for the DBO output, or if the instruction requires storage for a logic result, then the ACC (Accumulator Clock) on the processor timing card provides the timing.

Both DBC and ACC (if enabled) consist of a group of 32 pulses. DBC always occurs during the process frame; ACC may or may not appear during the process frame but will ALWAYS appear during the branch frame if there is a branch condition. If the cycle consists of four frames and ACC is enabled during the process frame, then ACC will appear as a group of 64 pulses, since it always occurs in the third frame (Branch Load frame) when four frames are generated in a cycle.

Branch Load Frame (Group C)

If the instruction read during the instruction read frame was a conditional branch, and if the branch condition was satisfied during the process frame, then a branch load frame is generated. During the branch load frame, data is shifted from MDO (Memory Data Output) through A18 on the instruction decode card to the accumulator. Timing for this transfer is provided by the ACC from the processor timing card.

The branch load frame should only be generated if Operator Output (OPO) and BNZ = CNZ = COX (conditional branch test signal) on the processor timing card go to a logic 1 for a full bit period during the process frame.

Increment/Load Frame (Group C or D)

The increment/load frame is an 8-bit interval, which follows either the process frame or the branch load frame.

Timing Oscillator

Refer to the computer block diagram in the student diagram book. The basic timing signals are derived from a 1 MHz oscillator on the processor timing card. This oscillator feeds six flip-flops. The six flip-flops are connected in such a manner that there are four outputs of 250 kHz. Each is different in phase. One output is fed through the clock and timing gating to Hexadecimal Counters to establish the basic timing; the Hexadecimal Counter, therefore, counts at a 250 kHz rate. The following signals are generated by the Hexadecimal Counters in reference to the following clock groups.

1. Clock group A (Instruction Read Frame) will always consist of 32 clock pulses and will generate the following signals.

INC (Instruction Storage Clock). This signal is required to load the instruction register from the specified hard-wire memory location.

IAC (Instruction Address Counter) Clock. This is used to increment the IAC counter. It consists of one pulse at count 30 of clock group A.

2. Clock group B (Process Frame) will always consist of 32 clock pulses and will generate the following signals.

ACC Clock (Accumulator Clock) will be generated conditionally upon bit 10 of the instruction word.

DBC (Data Bank Clock) will be generated at a 250 kHz rate during clock group B

3. Clock Group C and D

ARC (Address Select Clock) = 8 pulses. This clock has significance only during the execution of an OUTS instruction.

ACC (Accumulator Clock). This clock consists of 32 pulses in the event of a Branch condition.

SUMMARY

A read only memory (ROM) computer is the nucleus of the entire radio control group. The computer contains a unique hard-wired program that controls and monitors a complete radio group and a maintenance display unit.

The instruction decode card stores and decodes instructions and data received from the hard-wired memory card and routes data to and from the accessible memory according to the program instructions being processed.

The processor timing card provides the basic timing for the internal operation of the ROM computer.

There are three steps in the processor timing cycle:

1. Shifting the instruction data from the hard-wired memory into the instruction register.

2. Shifting the accessible memory data through gates, which have been enabled by the instruction decode and Op Code modifier bits.

3. Advancing the fixed wire module program to the next instruction in sequence by incrementing the IAC.

NOTES